NOSC TD 1092

NAVAL OCEAN SYSTEMS CENTER San Diego, California 92152-5000

NOSC TD 1092

Technical Document 1092
May 1987

Study and Development Effort on Opposed Gate-Source GaAs Devices

Cornell University
School of Electrical Engineering

Sponsored by
Defense Advanced Research Projects Agency
ARPA Order Number 4766

NAVAL OCEAN SYSTEMS CENTER

San Diego, California 92152-5000

E. G. SCHWEIZER, CAPT, USN
Commander

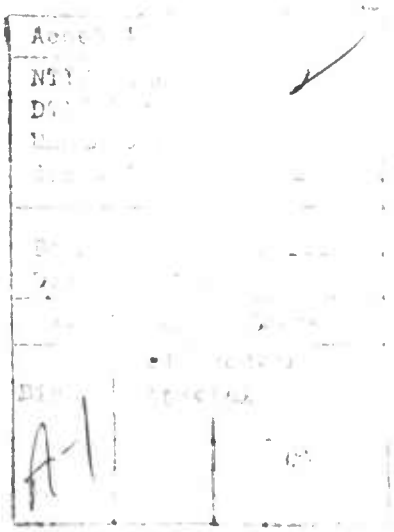
R. M. HILLYER
Technical Director

ADMINISTRATIVE INFORMATION

This work was performed for the Defense Advance Research Projects Agency, Arlington, VA 22209, under ARPA Order Number 4766. Work on contract N66001-83-C-0363 was carried out by Cornell University, School of Engineering, Ithaca, NY 14853. The Contracting Officer's Technical Representative was J.R. Zeidler, Code 7601, Naval Ocean Systems Center, San Diego, CA 92152-5000.

Released by
J.R. Zeidler, Associate for
Systems
Space Systems and Technology
Division

Under authority of
K.D. Regan, Head
Space Systems and Technology
Division



DISCLAIMER NOTICE

THIS DOCUMENT IS THE BEST QUALITY AVAILABLE.

COPY FURNISHED CONTAINED A SIGNIFICANT NUMBER OF PAGES WHICH DO NOT REPRODUCE LEGIBLY.

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

AD-A183 433

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release, distribution is unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S) TD 1092
6a. NAME OF PERFORMING ORGANIZATION Cornell University School of Electrical Engineering 6b. OFFICE SYMBOL (if applicable)	7a. NAME OF MONITORING ORGANIZATION Naval Ocean Systems Center
6c. ADDRESS (City, State and ZIP Code) Ithaca, NY 14853	7b. ADDRESS (City, State and ZIP Code) San Diego, CA 92152-5000
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Defense Advanced Research Projects Agency Defense Sciences Offices 8b. OFFICE SYMBOL (if applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER N66001-83-C-0363
8c. ADDRESS (City, State and ZIP Code) Arlington, VA 22209	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO: 61101E; PROJECT NO: DARPA; TASK NO: ARPA Order No. 4766; AGENCY ACCESSION NO: 1CEE 6BO

11. TITLE (Include Security Classification)
Study and Development Effort on Opposed Gate-Source GaAs Devices

12. PERSONAL AUTHOR(S)
C.A. Lee, K. Rauschenbach, J. Bellantoni, G.C. Dalman, H. Kondoh, A. Yarborough, J.P. Krusius, J. Nulman, A. Perera

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM Sep 83 TO Jun 86	May 1987	197

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Communications, Monolithic Arrays, Millimeter Waves, Surveillance, Opposed Gate-Source Transistor

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This document describes research on the Opposed Gate-Source Transistor (OGST) for the millimeter wave regime. Progress described concerns the development of self aligned lithography processes for fabricating a source contact opposite the gate electrode on a 200 nm GaAs membrane, the processing of an ohmic source contact, the fabrication of a Schottky gate contact compatible with the high temperature processing of the source contact, and the electrical characterization of the transistors.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS	UNCLASSIFIED

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL
J.R. Zeidler	(619)225-2030	Code 7601

DD FORM 1473, 84 JAN

83 APR EDITION MAY BE USED UNTIL EXHAUSTED
ALL OTHER EDITIONS ARE OBSOLETE

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

DD FORM 1473, 84 JAN

ABSTRACT

The objective of this program was to perform research on the Opposed Gate-Source Transistor (OGST) for the millimeter wave regime. This is the final technical report from this program. Progress described in this report concerns the development of self aligned lithography processes for fabricating a source contact opposite the gate electrode on a 200 nm GaAs membrane, the processing of an ohmic source contact, the fabrication of a Schottky gate contact compatible with the high temperature processing of the source contact, and the electrical characterization of the transistors. The analysis of the discrete device and distributed interaction operation was also carried out.

The goal of fabricating a working transistor was accomplished, but mounting in a microwave fixture degraded the performance so that positive gain at microwave frequencies could not be demonstrated. Probe measurements, however, showed oscillations if the gate and drain circuits were not properly terminated. Three types of lithography have been investigated, E-Beam, UV and X-ray. E-Beam and UV lithographies have been developed and used to make complete dual surface transistor structures on 200 nm membranes of GaAs with the requisite quarter micron electrode geometries. X-rays have been used to make a positive image of a 0.3 μm gate electrode on a 3 μm silicon membrane. Low frequency measurments have been obtained for these 200 nm membrane OGST's. For the demonstrated quarter micron source length made with 30 kV e-Beam lithography and with UV lithography the corresponding gate length of an equivalent conventional FET would be less than 0.25 μm.

Extensive computer modelling of the OGST structure has been carried out to evaluate the drain saturation and pinch-off, to show that the effects of asymmetry in the gate source fabrication are a mild degredation, to evaluate the interelectrode capacitances, to evaluate the step recovery time of the transistor, and to study the distributed interaction. All of these calculations support the view that the transistor should work well, as predicted, at 100 GHz. In addition, process simulations for dual surface lithographies have been carried out.

Finally, computerized vector and scalar network analyzers have been designed, constructed, and tested at Ka-Band and at W-Band. A W-Band waveguide to microstrip adapter supplied by TRW has been tested at W-Band and this design has been scaled to Ka-Band and tested.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION AND PROGRAM OBJECTIVES

The OGST design facilitates the reduction of parasitic inductances and capacitances between the intrinsic transistor and the external circuit that limit the frequency performance of the GaAs FET. In a conventional transistor design, using a lumped element approach, and assuming a total gate width of 100 μm for moderate power capability, the discontinuities between the input transmission line and the transistor will usually increase the input capacitance. In the conventional design of MESFET this parasitic capacitance can be an order of magnitude greater than the intrinsic gate-source capacitance. This increased input capacitance along with the source and gate inductances will generally resonate at a frequency much below 100 GHz. Another difficulty posed by the large gate width chosen for high power is the attenuation of the input signal along the gate line. A straightforward way of reducing this attenuation, and consequently reducing the source and gate line inductances as well as the gate resistance, is to parallel many gate and source fingers of a relatively short width. This solution, however, increases the difficulty of matching the gate and source to the input transmission line and leads to a larger increase of the gate-source capacitance. Parallelling many gate and drain fingers also leads to an undesirable decrease in the drain output impedance. The OGST design minimizes the electrode losses along the width of the device relative to all other designs. The principal limitation of most transistors is a large input capacitance several times that of the active gate electrode and a large source inductance for mm-wave operation even with via-hole construction. Thus the attainment of high power operation is severely

penetration for the source contact. A promising candidate for such a contact is one made of molybdenum germanide [1]. Only fragmentary descriptions of this contact exist in the literature and those descriptions were not consistent with our observations. As a consequence, extensive effort, in collaboration with Prof. G. Morrison of the Cornell Chemistry Department, has been made to characterize its properties for use in the OGST. In spite of the work invested in the Mo-Ge contact, the transistors were fabricated with a Au-Ge alloyed source contact [2] because the lower processing temperature of the Au-Ge substantially reduced the number of processing steps. Following the ohmic contact work, there are several subsections on device design, simulation and analysis of the OGST; this part also includes processing simulations. The final section of the report describes the computerized mm-wave network analyzers in Ka-Band and W-Band that were designed and constructed for characterization of the OGST. This section also describes the characterization of the W-Band waveguide-microstrip transition donated by TRW and the scaling and characterization of a Ka-Band version of this waveguide-microstrip transition. Finally, there is a description of the mounting and microwave testing of completed OGST's.

2. TECHNICAL RESULTS

2.1 DEVICE FABRICATION

2.1.1 OGST Processing Schedule

The transistor processing schedule is divided roughly into three main parts. The first part is devoted to fabrication of the gate structure on the active layer. Two approaches have been used for fabricating submicrometer gate lengths. One of these utilizes plating the gate in a channel that has been reactively ion-etched in a thick layer of polyimide; the other method directly etches the gate pattern in a 0.7 μm layer of tungsten using a carbon tetrafluoride plasma. The second stage of processing is concerned with etching an array of thin membranes that are approximately 80 x 100 μm and are aligned with the gate array by means of an infrared aligner. The third stage of processing deals with the fabrication of the source contact by a self aligned dual surface exposure through the active layer of the transistor.

Electrons, UV and X-rays have been investigated for carrying out the dual surface exposure. To evaluate the relative advantages of these exposure mechanisms one must consider the gate and source dimensions and the thickness of material through which the exposure must be made. The optimum OGST design calls for a source length that is about one half the gate length. The total thickness of material through which the exposure must be made may comprise 0.2 μm of GaAs, 0.1 μm of AlGaAs, 0.3 μm of polyimide, and 0.3 μm of a negative resist. In all this represents a thickness of some 0.9 μm for the X-rays, the electrons or the UV photons to travel. For X-rays this thickness presents no essential difficulty,

but obtaining a source image roughly half that of the gate length requires the use of some spacer technology which remains to be evaluated since X-ray lithography was only carried far enough to demonstrate a positive source image of the requisite dimension. Using electrons of the proper acceleration potential one can control the lateral spreading to achieve the desired source length in the self-aligned exposure as is illustrated in Fig. 1. We have also demonstrated that exposure control of UV and diffraction can be used to control the source image length to the required dimensions. For a strong X-ray source one must use a synchrotron source, while strong electron sources and UV sources are readily available. Process modelling for a total membrane and resist thickness of 1 μm had seemed to indicate that electrons of 100 kV would be necessary to fabricate a 0.25 μm source, but our investigations show that by utilizing exposure-contrast control a 0.25 μm source contact can be imaged using only the 30 kV electrons available in the Cambridge EBMF-2 microscope.

The common starting material for E-Beam, UV and X-ray processing was MBE grown wafers purchased from TRW (Dr. John Berenz). There are two epitaxial layers grown on a semi-insulating GaAs substrate. The first is an undoped layer of 1000 Å of $Al_{.3}Ga_{.7}As$, which is used as an etch stop layer, and the second is the active GaAs layer, which is 2000 Å thick with a donor density of $2 \times 10^{17}/cm^3$. The two inch diameter wafers received from TRW are cleaved into 8.8 x 8.8 mm chips. This size accomodates a 7 x 7 array of transistors and test sturctures located within a 7 x 7 array of 80 x 100 μm membrane windows to be etched in the substrate.

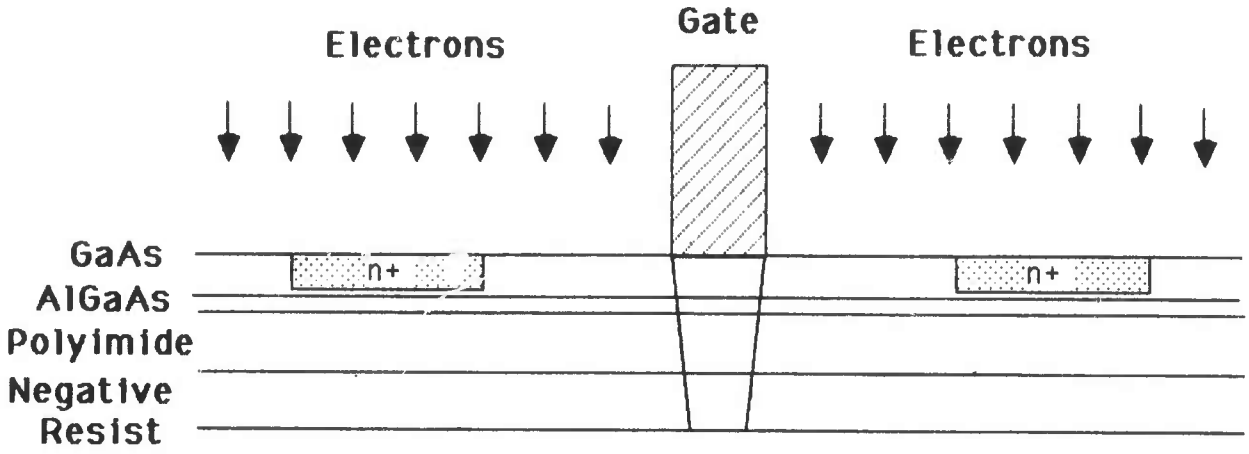


Figure 1 Schematic drawing of the self-aligned source exposure using electrons showing how the lateral scattering of the electrons narrows the source image relative to the gate electrode.

2.1.1.1 Fabrication of Membrane Array (K. Rauschenbach and C. A. Lee)

On the active layer of the cleaved sample, E-Beam lithography is used to define an array of implanted drain contacts and gate structures (the specific procedures for X-ray, E-Beam and UV dual surface exposures will be given in later sections). The sample with topside active layer contacts is then thinned to a thickness of 75μm and mounted on a sapphire plate. A polyimide etch mask is fabricated and registered with the gate electrodes on the semi-insulating side by the procedure given in Table I. To withstand the selective etch used to remove the substrate from the area of the membrane the polyimide etch mask must be hard baked. After such baking, however, it is very difficult to remove. With the etch mask in place, spin coating resist onto the membrane for the source lithography presents some difficulties in obtaining a uniform coating of the membrane. These difficulties prompted us to develop another masking procedure.

A much superior etch mask was developed that comprised some 400 Å of nickel which was patterned by conventional lithography to open up 80 x 100 μm areas in the nickel. Not only did the presence of the nickel improve the smoothness of the selective etch used to remove the substrate, but the coating was thin enough to wash away from the undercut area around the membrane. In addition, the thickness of the required nickel coating still permitted the etch mask to be registered with the gate electrode array with an infrared aligner. With the nickel etch mask and 75 μm substrates very uniform resist coatings could be spun onto the membranes for the source lithography.

Table I: Processing Schedule Etching for Thin GaAs Membranes

(K. Rauschenbach, and C. A. Lee)

I. Scribe wafer into desired geometry (e.g. 9 mm by 9 mm squares).

II. Lap samples to uniform thickness, 10 mils.

III. Polish samples to approximately 3 mils depending on the dimensions of the window.
   1) A standard solution of Clorox is adequate for polishing.
   2) Polish with a force of about 100 gm/cm^2.

IV. Mounting of Samples for Etching.
   1) On an optically polished sapphire disk, spin on Ciba-Geigy polyimide.
   2) Place the GaAs sample onto the partially dried polyimide film.
   3) Cure the polyimide cementing the sample to the sapphire disk under the following conditions:
      a) Bake at 80 °C for 30 min.
      b) Bake at 150 °C for 15 min.
      c) Bake at 225 °C for 15 min.
   4) Immediately after the sample has returned to ambient temperature begin fabricating the etch mask as described in step V.

V. Fabrication of the Polyimide Etch Mask.
   1) Preparation of Pyralin adhesion promoter.
      a) Mix a solution of 0.05% DuPont Pyralin VM651 organo-silane diluted with 90% methanol and 10% de-ionized water. Allow 24 hours for reduction.
   2) Apply adhesion promoter and spin at 5000 RPM for 60 seconds.
   3) Spin on DuPont Pyralin PI-2555 at 5000 RPM for at least 60 sec.
   4) Partial imidization of the PI-2555 is accomplished as follows:
      a) Stabilize the oven temperature 1 hr at 137 °C.
      b) Bake sample at exactly 137 °C for exactly 30 min.
      c) Let sample return to room temperature before proceeding to the next step of vapor phase priming.
   5) Vapor phase priming for the mask:
   6) Spin on Shippley S-1400-31 at 5000 RPM for 60 sec. This yields a film thickness of approximately 2 μm.
   7) Soft bake the photoresist at 90 °C for 30 min after oven temperature recovery.
   8) Expose the etch mask pattern in an infrared aligner to register the 80 x100 μm openings with the array of gate contacts on the other side of the wafer. Adjust the exposure energy for a development and etch time of 60

sec.

9) Spin-spray develop the sample. Calibrate air pressure in the spray nozzle and the RPM of the spinner for uniform development and etching.

10) Cure the etch mask according to the following schedule:
    a) Bake at 300 °C for 30 min.
    b) Bake at 400 °C for 30 min.
    c) Bake at 450 °C for 10 min.

    This schedule will fully cure the polyimide etch mask.

VI. Jet Etching of Thin Membranes.

1) Use a selective etch solution composed of 30% hydrogen peroxide and ammonium hydroxide to etch the GaAs substrate down to the $Al_xGa_{1-x}As$ stop layer. Experiments were performed on the GaAs-AlGaAs interface to determine an etch concentration which maximizes selectivity while still producing a polished and uniform surface. The optimum mixture was found to be a 25:1 solution of 30% hydrogen peroxide and ammonium hydroxide adjusted to a pH of 8.4. This etch has been successfully used with stop layers with the aluminum concentration, x, in the range of 0.3 to 0.5.

2.1.2 Device Processing Schedule Using X-ray Lithography

(J.P.Krusius, J. Nulman, and A. Perera)

In the exploratory process simulations described in Sec. 2.2.1 it was found that x-rays allow the thickest membranes and provide the smallest feature sizes in self-aligned dual surface lithography. Contrary to conventional x-ray lithography, which is mainly limited by geometrical image distortion (penumbral blur, lateral magnification error), and layer to layer registration, self-aligned dual surface lithography is primarily constrained by the range of x-ray generated photoelectrons. This is of the order of 20 nm. 200 nm wide backside lines in PMMA have been demonstrated in this work with membranes as thick as 3 μm. With x-rays it is thus be possible to to align the gate and source lines ideally with no offset and an undercut of only 20 nm per edge. It is anticipated that self-aligned dual surface x-ray lithography will have future applications in microfabrication well beyond the OGST.

2.1.2.1 Demonstration of Self-Aligned Dual Surface Lithography

Self-aligned dual surface X-ray lithography has been demonstrated in this work for the first time. Since no past experience was available it was decided to perform this demonstration with relatively thick silicon membranes prepared by wet chemical etching using a heavily boron doped surface layer as the etch stop. Membranes in Si are easier to make than in GaAs, and they are mechanically much easier to handle in further processing, and can be made much thicker than GaAs membranes. Here about 3 μm thick large area membranes were used.

A brief overview of the demonstration process is given in Table II. A detailed process schedule can be found in Appendix I. Arrays of 3 μm thick 6 mm x 6 mm wide membranes were fabricated on silicon wafers using boron predeposition and selective chemical etching with pyrocathecol. Si_3N_4 was used as the diffusion and etch mask. The top surface X-ray absorber mask is made using Au electroplating into resist windows. Pattern definition was accomplished with direct electron beam writing on the high resolution tri-layer resist PMMA/SiO_2/Polyimide [3]. The resulting resist image written with the Cambridge EBFM2-150 pattern generator is shown in Fig. 2, the electroplated line prior to resist removal in Fig. 3, and the final electroplated top side 600 nm thick Au absorber mask line in Fig. 4. The X-ray exposure was performed with Cu_L X-rays produced by bombarding a copper plate in vacuum with electrons with an energy less than 6 keV with the exploratory X-ray system at the National Submicron Facility. Fig. 5 shows an overview of such back side PMMA lines on the Si membrane. The lines and spaces are 300 nm and 500 nm wide respectively. Fig. 6 shows the cross section of a back side resist line profile on the Si membrane after cleaving. A sharper image is difficult to obtain because of the thin resist and its charging during SEM inspection. The line width is about 200 nm and the aspect ratio about 2:1. Walls are vertical. This linewidth corresponds to the minimum linewidth of the top surface Au absorber. The self-aligned undercut induced by the X-rays appears very small, although no systematic measurements of it have yet been made. More details are given in Ref. [4].

The above demonstration thus clearly shows that the developed self-aligned dual surface x-ray lithography exceeds both minimum

Table II. Process Outline for Self-Aligned Dual Surface X-Ray Lithography.

Step	Description
1	define membrane
2	evaporate 50 A Cr and 150 A Au to form plating base
3	spin on 1 μm polyimide (Ciba Geigy XU285), deposit 300 A SiO_2 interlayer using plasma enhanced CVD, spin on 1500 A PMMA to form tri-layer resist structure
4	expose with Cambrige EBMF2-150
5	develop image in PMMA, transfer image through SiO_2 and polyimide using reactive ion etching with CHF_3 and O_2
6	electroplate Au to thickness of 8000 A (SelRex BDT 500)
7	strip resist layer
8	ion mill excess plating base (Ar, 500 eV)
9	spin on 1500 A PMMA resist on back side
10	expose with Cu_L X-rays
11	develop back side image

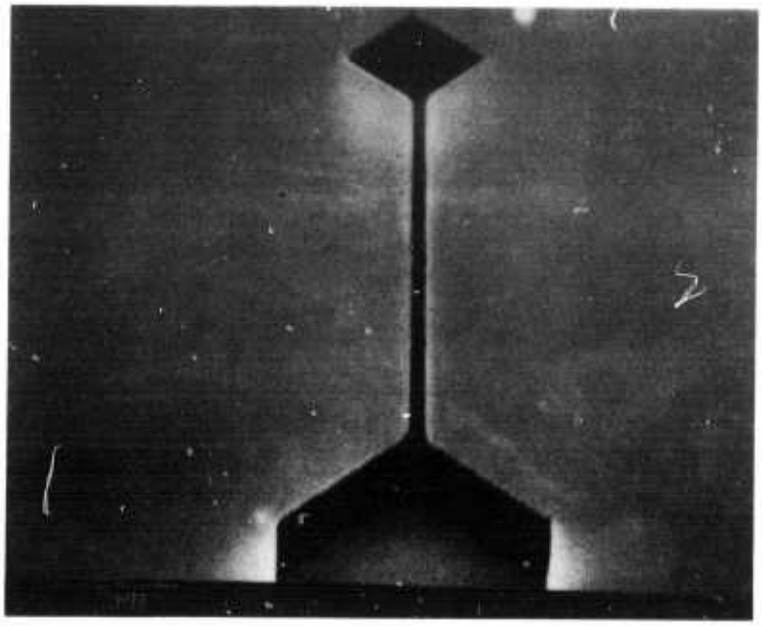


Figure 2 Tri-layer gate level resist image after complete pattern transfer.

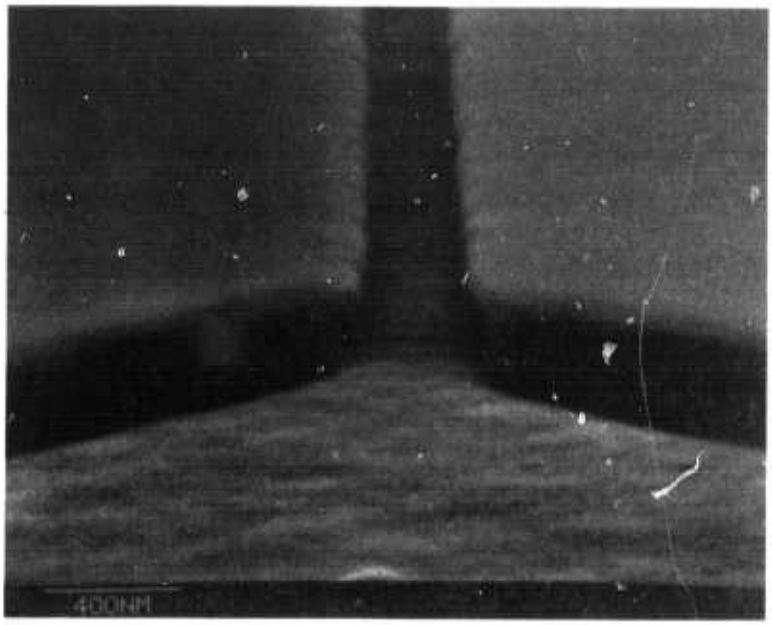


Figure 3 Electroplated gate line after completion of plating.

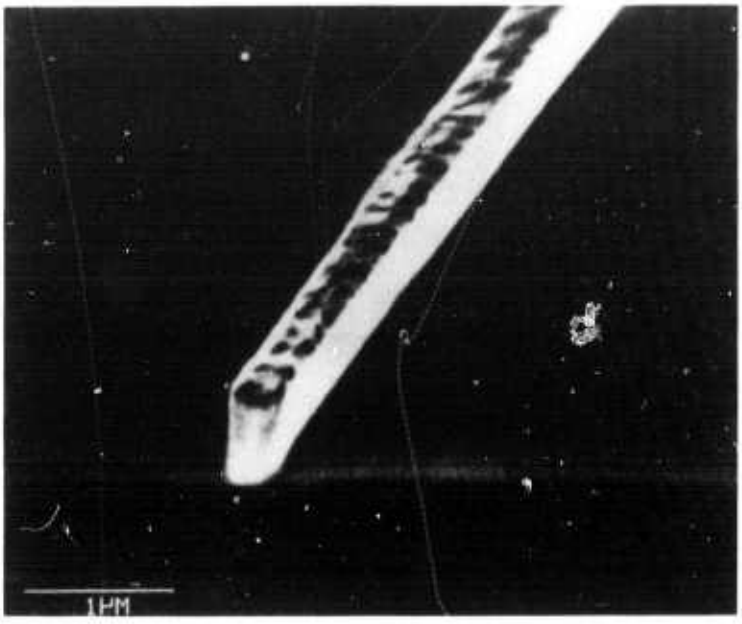


Figure 4 Micrograph of 300 nm wide Au X-ray mask line with an aspect ratio of 3:1.

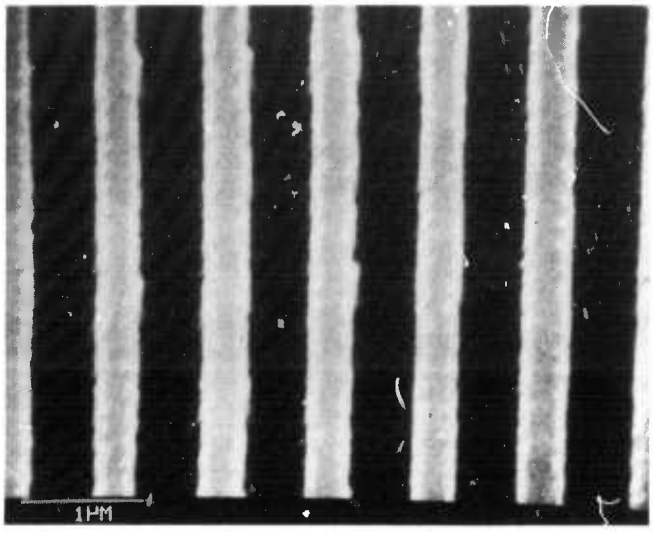


Figure 5 Micrograph of developed back side PMMA layer under the Si membrane. PMMA lines have a light appearance.

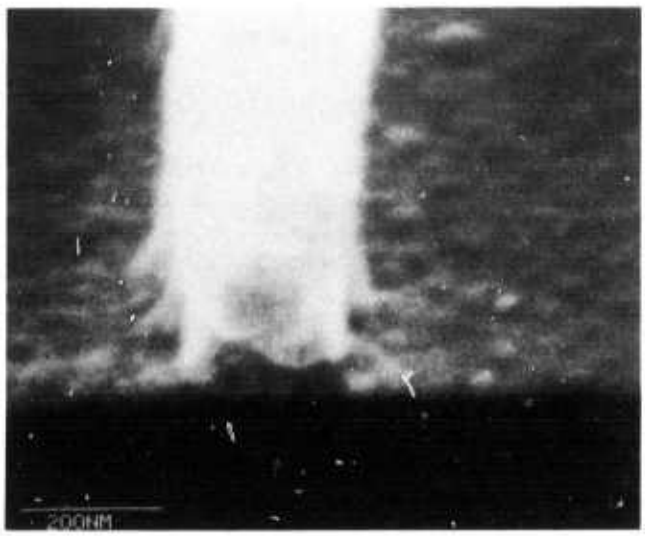


Figure 6 Micrograph of cleaved back side PMMA line on top of the Si membrane. The width of the line is about 200 nm and the aspect ratio 1:1.

linewidth and alignment requirements defined by the millimeter wave OGST.

2.1.2.2 Integration of Self-Aligned Dual Surface X-Ray Lithography into Fabrication Process

In the following discussion we will show how the above novel self-aligned dual surface x-ray lithography can be applied to make millimeter wave OGST devices with an ideal symmetric structure. Two approaches to process integration have been considered, which differ in the realization of the thin substrate regions needed for the self-aligned dual surface lithography. The first one is based on selective thin membrane areas etched into a thicker substrate. Complete substrate removal with membrane islands supported by a suitable support structure constitutes the second approach. In both cases the same fabrication steps are used for the top surface gate and drain electrodes.

The starting material consist of 2000 A GaAs and 1000 A AlGaAs films grown by MBE on semi-insulating (S.I.) GaAs substrates. First the gate areas are defined as follows. 2000 A of TiW gate metal is first sputter deposited followed by an evaporation of 50 A of Cr and 200 A of Au. The latter two materials are needed as a plating base for subsequent Au electroplating. Next a tri-layer high resolution electron beam resist structure [4] composed of 1.0 μm polyimide, 400 A of plasma enhanced CVD SiO_2, and 1500 A of PMMA is applied on top of the existing composite Au/Cr/TiW film. Then the gate level image is written into the top PMMA layer with electron beam direct writing. After developing the exposed patterns and succesive image transfer through the SiO_2 and polyimide

using reactive ion etching (RIE) in CHF_3 and O_2 ambients respectively (Fig. 2), Au is electroplated to a thickness of 8000 A (Fig. 3). The BDT-510 electrolyte [5] was chosen as the Au source, since it does not erode the plating mask and produces stress free films at a deposition rate of 2000 A/min at a 50 C bath temperature. After stripping the organic resist in O_2 plasma, and Ar ion milling is used to remove the excess plating base. The TiW layer was finally etched with CF_4 RIE. The ohmic drains contacts are then defined by conventional optical lithography and conventional Au:Ge contact metallurgy. An alternative is to define the drain areas after the source. This completes the fabrication of the top surface structures.

In the first approach for the self-aligned dual surface x-ray lithography (devices on thin membrane areas, see Fig. 7) an infrared aligner is used to define the membrane area from the back of the wafer. This alignment is non-critical. A selective etch of the S.I. GaAs substrate with the AlGaAs acting as a stop layer follows. A mixture of hydrogen peroxide and ammonium hydroxide is used as an etch. A thin layer of Si_3N_4 is then deposited onto the back surface. Subsequently the high resolution resist PMMA resist is spun on the back surface. With a substrate thinned down to 1-2 mils a reasonably uniform resist coating should result. In the second basic appraoch (substrate removed device, see Fig. 8), the wafer is mounted on a metal ring with a glass support using polyimide. The S.I. GaAs is then selectively removed with a wet etch. A CVD Si_3N_4 film used for passivation is then deposited and PMMA resist spun on the back side. In this approach PMMA has to cover a much shallower structure than in the first case (2000-5000 A), and thus a

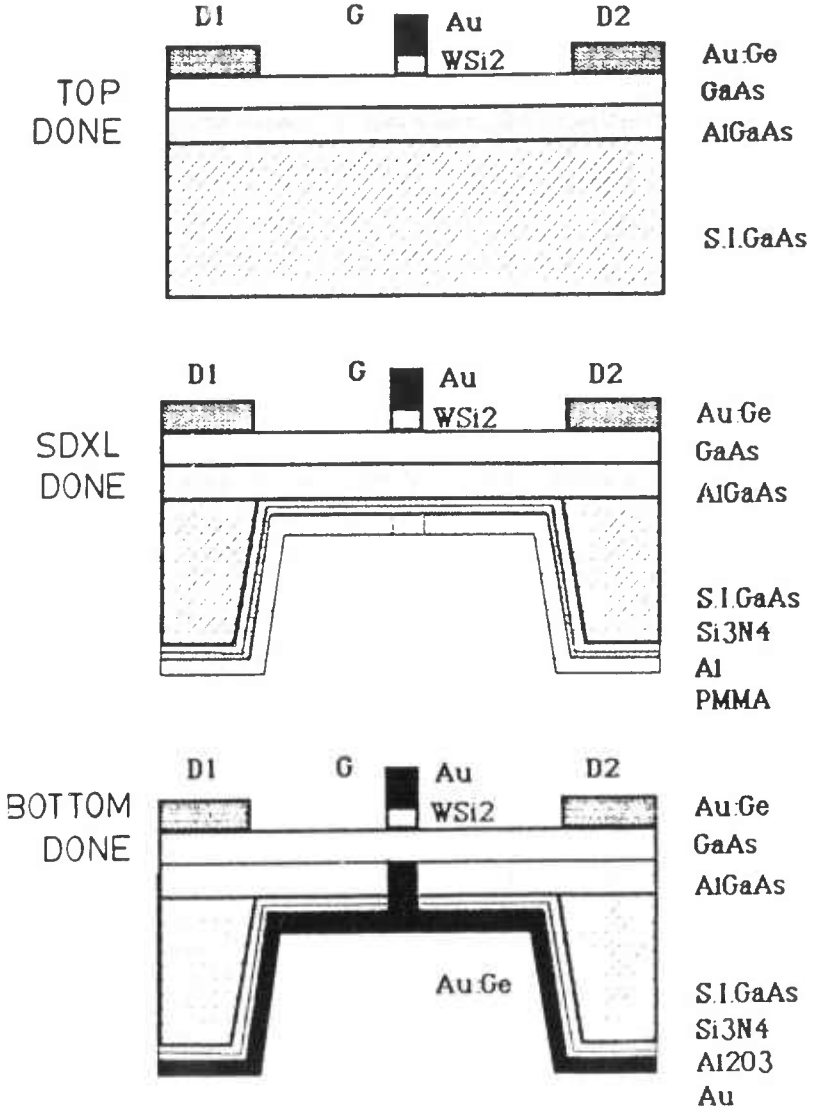


Figure 7 Process sequence for membrane type OGST devices.

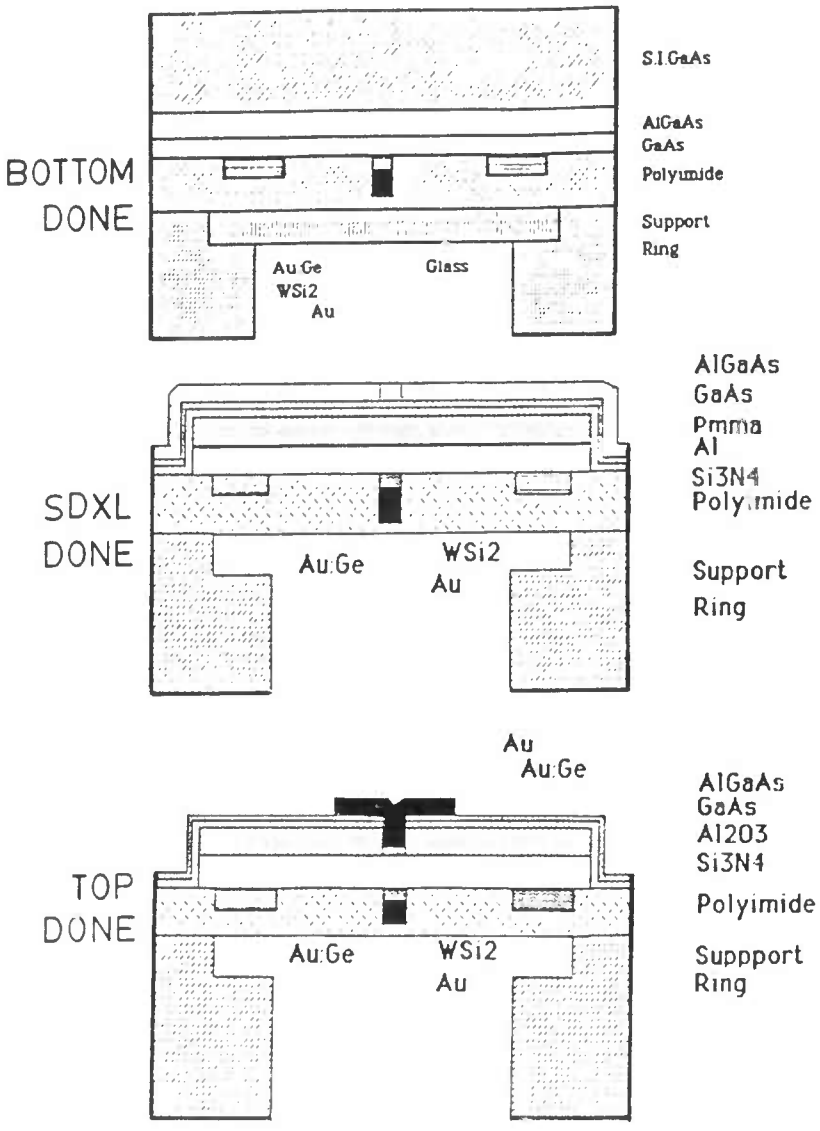


Figure 8 Process sequence for substrate removed OGST devices.

more uniform coating will obtained. Backside materials and layer thicknesses are subject to change pending on the findings of the phase matching conditions for distributed interaction (Sec. 2.2.2).

Soft x-rays, such as the Cu_L line, are then in both cases used for the self-aligned back side resist exposure. An example of such an exposed and developed 2000 A wide line in 1500 A back side PMMA resist is shown in Fig. 6. Aluminum lift-off, or local plasma oxidation a substitutional aluminum layer [6], is then used to invert the source pattern. Pattern transfer through the $Si3N_4$ and the AlGaAs layers to the active GaAs layer is accomplished with RIE. A film deposited via plasma enhanced CVD followed by anisotropic RIE can be used to trim the width of the source electrode line to a value given by device design. This technique is the inverse of outside spacers often used e.g. for self-aligned short gate MOS devices. For the above device dimensions an inside spacer layer thickness of about 800 A is needed. Finally an Au:Ge source metal contact layer is deposited and alloyed using rapid thermal annealing in order to minimize erosion of the active layer. Finally back surface metal ground plane is evaporated.

2.1.2.3. Layout Design of OGST Test Chip

A test chip based on mixed optical projection lithography and electron beam direct write lithography has been designed. The chip measures 6.5 mm x 6.5 mm with a 2x2 array of 3.2 mm x 3.2 mm electron beam subfields. The optical lithography covers the full chip area. The layout design includes a total of six layers to be patterned. Electron beam lithography is used for gate and drain levels only (Table III). The

Table III. Mask Levels of OGST Chip

Level	Label	Lithography	Color
1	Gate	E-Beam	Red
2	Membrane	Optical	Black
3	Source	X-Ray	Unspecified
4	Drain	E-Beam	Blue
5	Isolation	Optical	Orange
6	Metal	Optical	Purple

source level is accomplished with self-aligned dual surface x-ray lithography. The remaining layers defined with optical projection lithography are as follows: membrane definition, device isolation, and global metal for pads. Membranes of 100 μm x 80 μm size were placed on a 1 mm square grid in each subfield. 70 different test structures and OGST's were placed on the 36 membranes. The OGST array with 36 different devices had gate lengths from 0.3 to 1.0 μm and gate width of 40 and 70 μm. The 24 designed test structures were loosely coupled OGST type gate and drain microstrip lines with similar widths and lengths and are intended for characterization and parameter extraction on the network analyzer. Typical layouts of OGST devices and microstrip lines are shown in Fig. 9 and 10.

2.1.2.4 Process Schedule for Membrane Devices Based on Self-Aligned Dual Surface X-Ray Lithography

The fabrication process based on etched membranes (Sec. 2.1.2.2) and self-aligned dual surface lithography (2.1.2.1) has been explored further. All patterning was performed according to the layout described in Sec. 2.1.2.3. A process run was started late 1985. The detailed process schedule is given in Appendix II. The run was delayed for several months because of the unavailability of the electron beam pattern generator. A chip, with the process completed until the gate level, were ready for membrane etching mid April 1986. The membrane etching has not been completed, and hence this process has not been explored further yet.

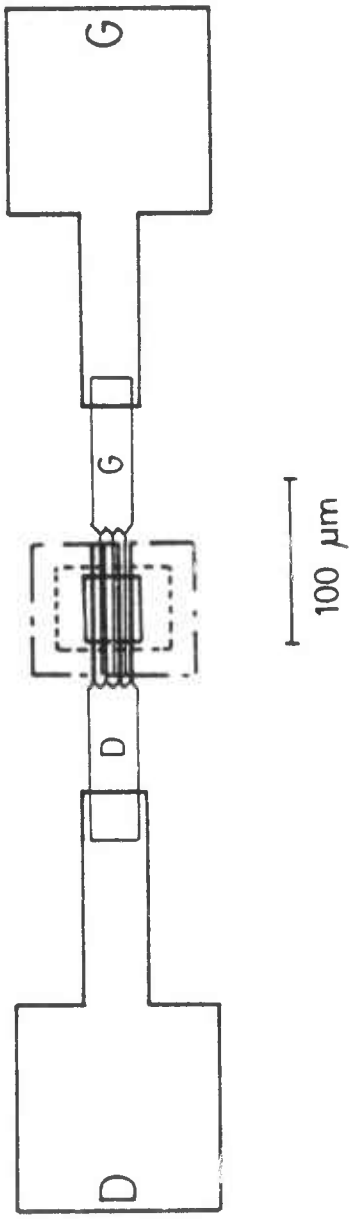


Figure 9 Typical layout of OGST device with three paralleled gate fingers.

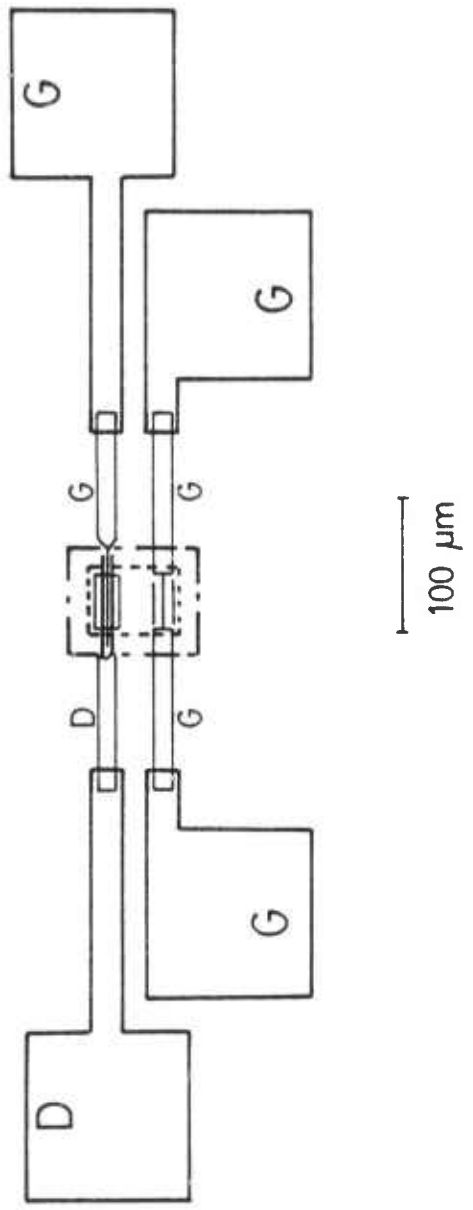


Figure 10 Typical layout of gate-line type microstrip test structure and OGST with two gate fingers on same membrane.

2.1.3 Device Processing Schedule Using E-Beam and UV Lithography

(K. Rauschenbach, C. A. Lee)

2.1.3.1 Gate, Membrane and Source-Image Fabrication and Evaluation

A number of changes are introduced in the processing by using electrons for the dual surface self-aligned exposure. Some of these differences are fundamental such as the ability to use a negative resist for the self-aligned exposure and to use the electron scattering in the membrane plus the resist layers on it to obtain a source length that is about half that of the gate electrode. Simulations of the energy deposition of high voltage electrons indicated that fabrication of the submicrometer millimeter-wave structure would require 100 kV electrons when lateral scattering through several layers of semiconductor and resist were accounted for. Our experiments demonstrate, however, that 30 kV electrons, available in the EBMF2 microscope, are sufficient for fabricating source images of less than a quarter micrometer. The explanation lies in the high contrast of the resist and control of the exposure used for the dual surface lithography. We have shown that a two to one ratio of gate to source lengths can be attained for 30 kV electrons if the gate electrode is some 500 nm long. With these dimensions, which are equivalent to a 250 nm gate length in a conventional FET, the self aligned source fabrication process by E-beam exposure is simpler and can be carried out in an instrument with a high degree of control over the exposure process. We have also demonstrated that dual surface self aligned UV exposures can be controlled in a similar manner to yield the required resolution for a quarter micron source image. It may seem surprising that a resolution in the quarter micron range can be achieved

with UV exposures, but it must be remembered that in the dual surface exposure the mask is conformal and the very high refractive index of the membrane reduces the effective wavelength thus limiting the edge diffraction to much less than is possible with normal contact printing.

For E-Beam and UV processing, a 7 x 7 array of gate structures and drain contacts are made as shown in Fig. 11. The drain contacts are implanted through a mask, but are not metallized until later in the processing because the metallization would interfere with the dual surface exposure. The gates in this array are of different lengths, from 0.25 to 2.0 μm in order to yield information on the exposure control and resolution of the dual surface self-aligned exposure. The dotted line surrounding the active area in Fig. 11 is formed late in the processing and serves to eliminate some end effects on each transistor and to isolate each transistor in the array, but in the transistors fabricated to date this refinement has been dispensed with.

To fabricate the gate electrodes a 700 nm film of tungsten is sputtered over the entire 9 x 9 mm wafer. On top of the tungsten there is a 30 nm overlayer of nickel. PMMA is spun onto the nickel and the positive gate patterns are exposed in the EBMF2. The nickel in the gate patterns is oxidized and the resist and remaining nickel are removed. The negative gate patterns are then reactively ion-etched. Figure 12a shows a 0.2 μm gate of foreshortened height and Fig. 12b, which is an end on view of the tungsten layer shows the height to be 0.6 μm. The gas used in the reactive ion etching was CF_4. Previous reports [7] had indicated that the undercutting was severe when gratings were etched with this gas , but with only a single line the undercutting or overcut-

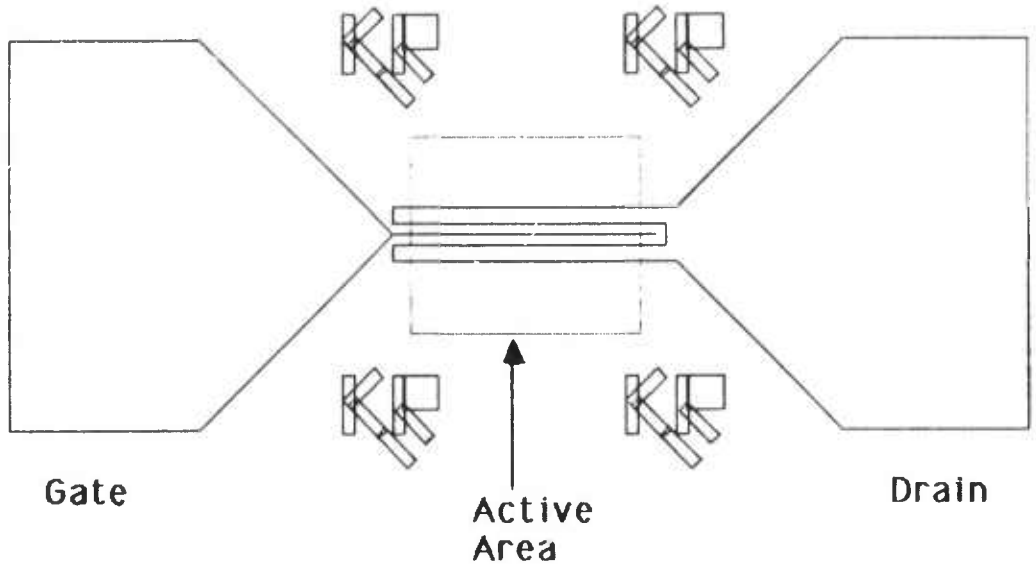


Figure 11 Layout of the gate, and drain electrodes with contact pads. The dotted line shows the active area of the transistor and the membrane area is just slightly larger, about 80 x 100 μm.

a)

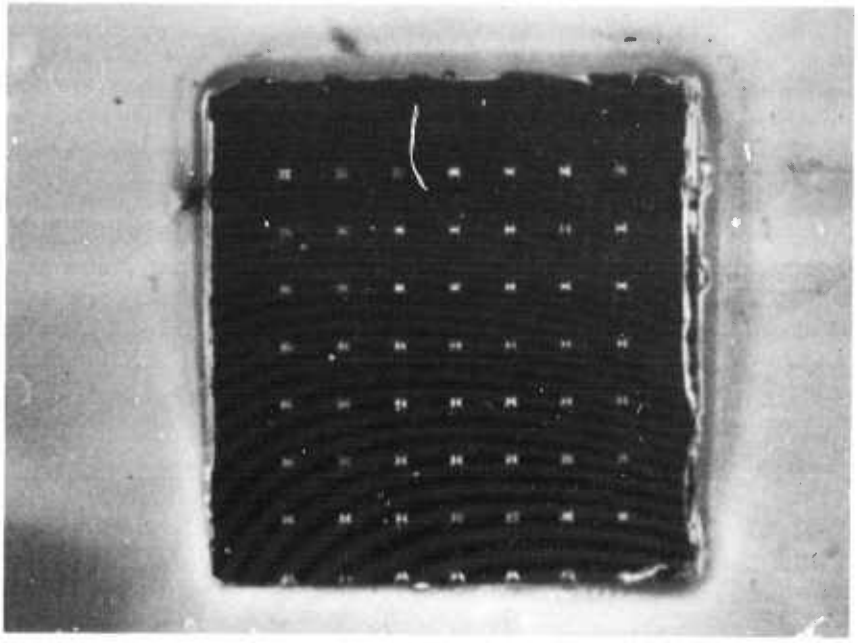
b)

Figure 12 a)SEM photograph of a 0.2 μm wide tungsten gate electrode; b)end on view of the tungsten layer to determine the height of the gate electrode in a) which is foreshortened by the angle of viewing.

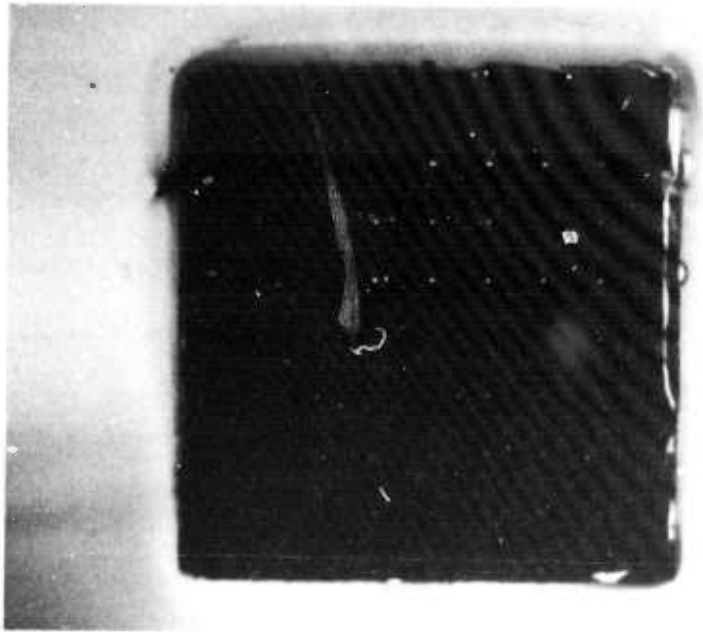
ting can be controlled by the gas pressure and the rf power. This reactive ion etching procedure is simpler and less critical than plating the lines in a channel.

After fabricating the gate array the wafer is then thinned down on the semi-insulating side and mounted on a sapphire disk in preparation for making the etch mask according to the procedure described in Table I. It was observed that after the high temperature baking of the mask (step V.10 of Table I), which was necessary for the mask to withstand selective etching of the semi-insulating GaAs, the sample with the membranes was sometimes difficult to remove. This problem was overcome by removing the sample from the sapphire disk before baking the mask at high temperature. Later use of a nickel etch mask simplified this procedure by eliminating the need for hard baking of the mask. Figure 13a shows the wafer after etching the membranes as viewed from the semi-insulating side and in incident light. Figure 13b shows the same view of the wafer except that the illumination is mostly transmitted light enabling one to view the transparent membranes. The aluminum concentration of the stop layer was only 30% and the thickness was only 100 nm, which is on the borderline for selectivity of the etch between GaAs and AlGaAs. Nevertheless, the yield of usable membranes was routinely greater than 90%, barring any defects in the MBE wafer. Both the polyimide and the nickel etch masks were sufficiently stable to withstand the hot hydrofluoric acid bath used to remove the AlGaAs stop layer.

The next objective was to image the gate electrode in a negative resist on the opposite side of the membrane. The choice of a negative



a)



b)

Figure 13 a)Optical view of wafer after etching the membrane array as viewed from the semi-insulating side of the wafer in incident light; b)the same view with predominately transmitted light to show the transparency of the membranes.

resist that had submicrometer resolution centered on a Novolac resist (Shipley 2415) that contained an additive with the property that electron exposure destroyed the ultraviolet sensitivity of the resist [8]. This resist is capable of making a submicrometer negative image of the source electrode by exposing it to electrons going through the membrane, then exposing the resist to UV radiation incident on the semi-insulating side of the wafer and developing the source image. There is a further restriction, however, in the requirement that one be able to etch away the AlGaAs layer after making the negative source image. Since the Novolac resist will not withstand this etch, a layer of cured polyimide is spun on to the membrane before putting on the negative resist. This procedure will give about the same etch resistance as we obtained with the membrane etch mask. An alternative procedure here is to remove the AlGaAs layer before spinning on the polyimide and Novolac resists thus avoiding the requirement of hard baking the polyimide.

The requirement that electrons must pass through the membrane means that the membrane with the Novolac resist and the polyimide be removed from the sapphire disk without altering its properties. Thus the wafer must be remounted on the sapphire disk with a material whose solute will not affect the Novolac resin. A number of water soluble compounds were found suitable including gelatin and glue. The remounted wafer with membranes is coated with polyimide and then with the Novolac resist. It is then removed from the sapphire disk, cured and exposed to 30 kV electrons in the EBMF2. This electron exposure is a masked exposure in that the electron exposure is confined to the immediate area of the electrodes as shown in Fig. 11. Since the electron exposure must be in the

range of $10^{-5} C/cm^2$, exposing the entire wafer leads to very long exposures of hours in length; confining the exposure reduces the time by about two orders of magnitude. After the electron exposure the wafer is remounted on the sapphire disk for development of the source image.

The new UV process developed for fabricating OGST's uses a relatively new photo-imagable polyimide, Probimide 337, which is a negative working resist with extremely high contrast. After etching the membranes and removing the AlGaAs stop layer the Probimide may be spun onto the membranes and the supporting substrate. The source image may now be exposed after giving the resist a recommended baking cycle while the membrane is mounted on the sapphire substrate.

For UV irradiation one should use the 436 nm line of mercury. The importance of using this resonance line is that it is close to the E_1 absorbtion line of GaAs ($L^V_{4,5}$ to L^C_6) and in the neighborhood of this absorbtion resonance the relative diectric constant of GaAs rises to a maximum value of 25 [9]. The transparency of the membrane, moreover, is well within the exposure range of the resist. As a consequence of these properties of the GaAs, the wavelength of the UV radiation inside the semiconductor is less than 900 Å while the gate dimensions that are being replicated are three to six wavelengths of the radiation. This utilization of the reduced wavelength of the UV radiation within the GaAs at a resonant absorbtion in conjunction with a very high contrast negative working Probimide resist are the key points in understanding how quarter micron source electrodes can be fabricated in an OGST with 436 nm UV radiation.

At this stage of the process development a considerable time was spent trying to obtain a good photograph of the source image. Optical photographs such as the one shown in Fig. 14 clearly show a resist image for gross features such as the gate pad but the fine line of the desired source image is barely visible. In transmitted light, as shown in Fig. 15, a clear image of the gate can be seen, but no details of the source image are visible. Several attempts to obtain SEM pictures of the membrane showed no details even when coated with 50 - 100 Å of gold or platinum. Assuming that charging effects were responsible, the membrane was embedded in silver paint and the resulting SEM picture is shown in Fig. 16a. Athough the membrane is covered with a 200 Å sputtered gold film, the edge of the etched membrane, the silver paint beneath the membrane, and the gate metallization are clearly visible, but no details of the patterned resist on top of the membrane are visible. A magnified view of this same membrane, Fig. 16b, shows no further details except that the gate length is about 1.2 μm.

Our understanding of the problem at this point was that the membrane was far more transparent to electrons from the SEM than had been expected. To remedy this unexpected transparency we doubled the sputtered gold coating to 300 Å and the result is shown in Fig. 17. This figure shows a high reflectivity from the top surface, remnants of the etch mask and from the gate metallization underneath the membrane. Incidentally, the membrane in this photograph was etched with a nickel mask; the nickel mask in this case was thicker than necessary so that it did not wash away in the etching process along the upper three sides.

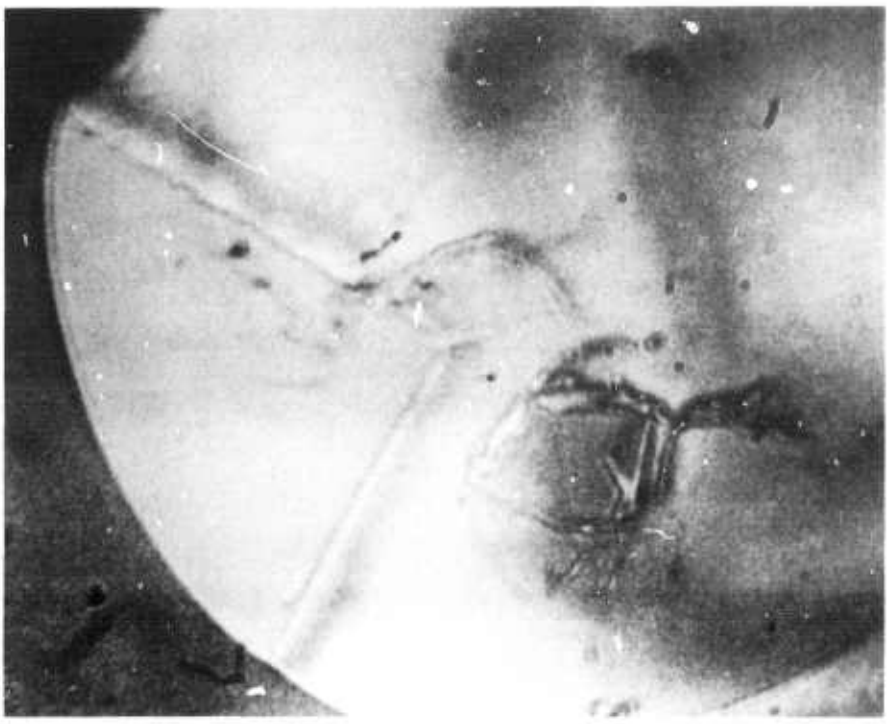


Figure 14 Optical photograph of source electrode image in negative resist obtained by electron exposure through the membrane. The triangular part of the contact pad is easily visible, but the source image in the active area is barely visible.

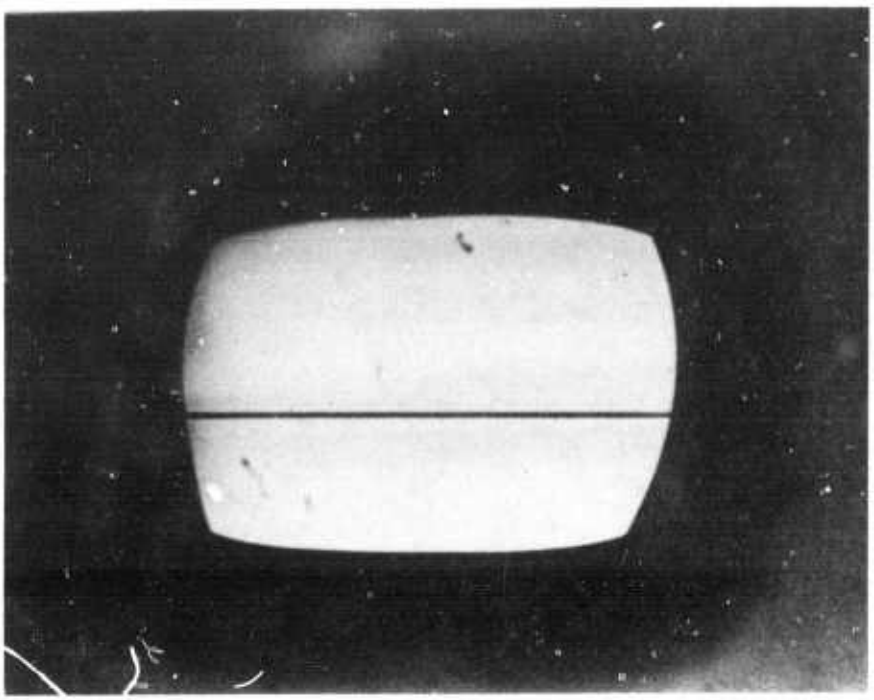


Figure 15 Optical view of the gate electrode on a membrane seen in transmitted light.

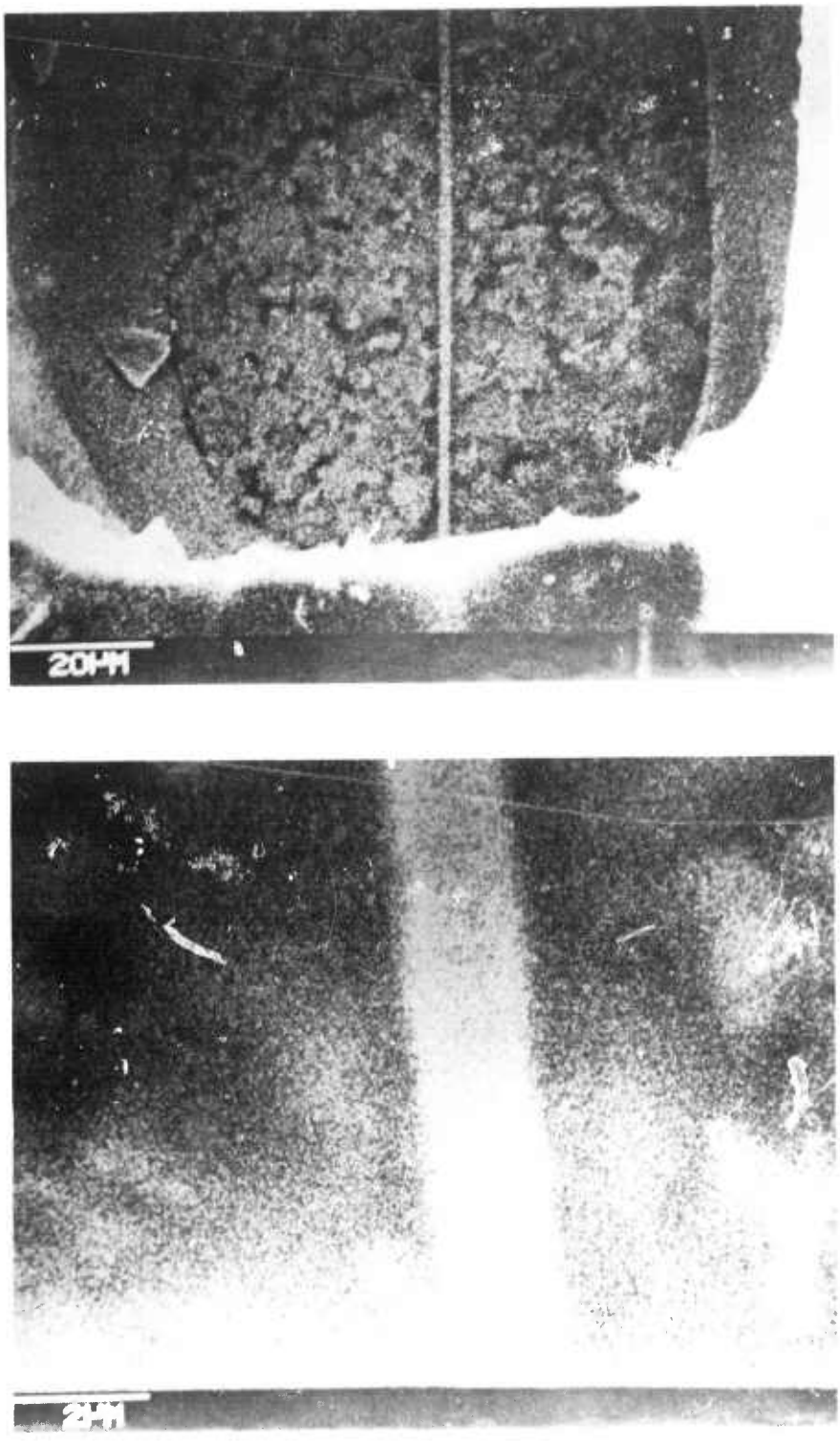


Figure 16 a)SEM photograph of membrane with a gate electrode and a developed source image on the side toward the viewer. The granular material on either side of the gate is silver paint used to suppress charging effects. The source image is quite transparent. b)A magnified view of a).

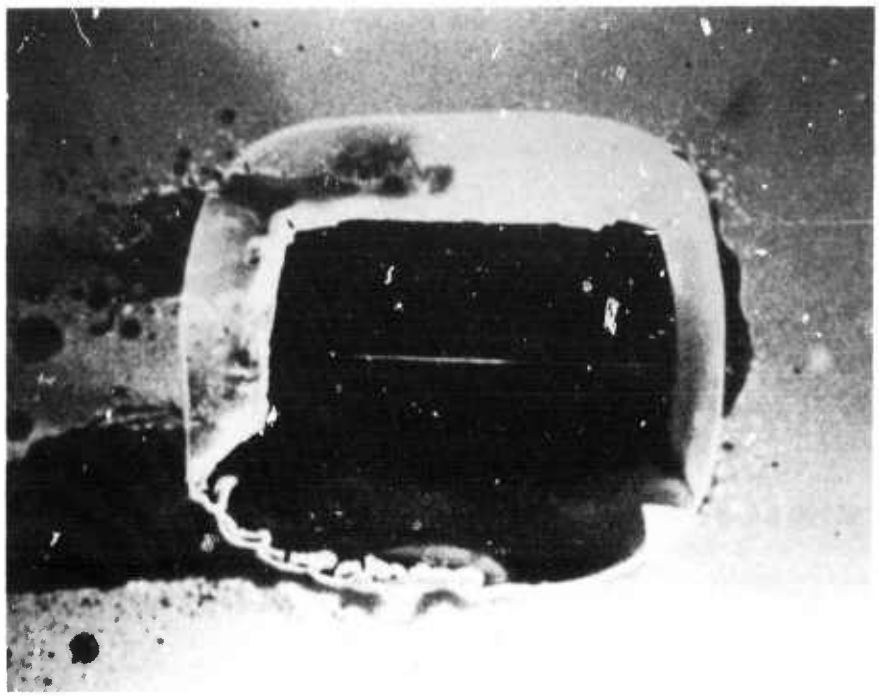


Figure 17 An SEM photograph of a developed source image with a 30 nm overlayer of gold still failing to show the source image.

To increase the reflectivity of the membrane the gold coating was increased to 600 Å and the sample was tilted to enhance the brightness of the relection from the membrane. Figure 18 shows the image of a 1 μm gate with this 600 Å coating. The electrons are incident on the membrane at an angle from the vertical d towards the bottom of the picture. Note that the lower edge of the source image is much brighter than the upper edge. This brightness difference is caused by the fact that electrons hitting the lower edge will hit the tungsten gate beneath the membrane and be reflected while electrons incident on the upper edge go right through the membrane into the supporting medium and are not reflected. Thus the upper edge looks dark. The image of a 2 μm gate is viewed along the length in Fig. 19. Here the electrons are incident on the membrane from above and to the left, making the left side of the image brighter. The white region at the bottom third of the photograph is the semi-insulating edge of the etched region. Electrons which go directly into the source region will go through the resist and the unbacked membrane and since they are not reflected no details at the bottom of the source image are possible.

At this stage, some feeling was developed for the transparency of these membranes with resist images and thin gold overlays. Another sample was prepared with about 1 μm of polyimide and 1600 Å of gold was deposited over the source image. Figure 20 shows an oblique view of a membrane and although there are obviously adhesion problems with the polyimide they are actually helpful for orientation. The electrons are incident from an axis tilted from the vertical towards the top of the picture. The picture is viewed from a direction tilted opposite to the

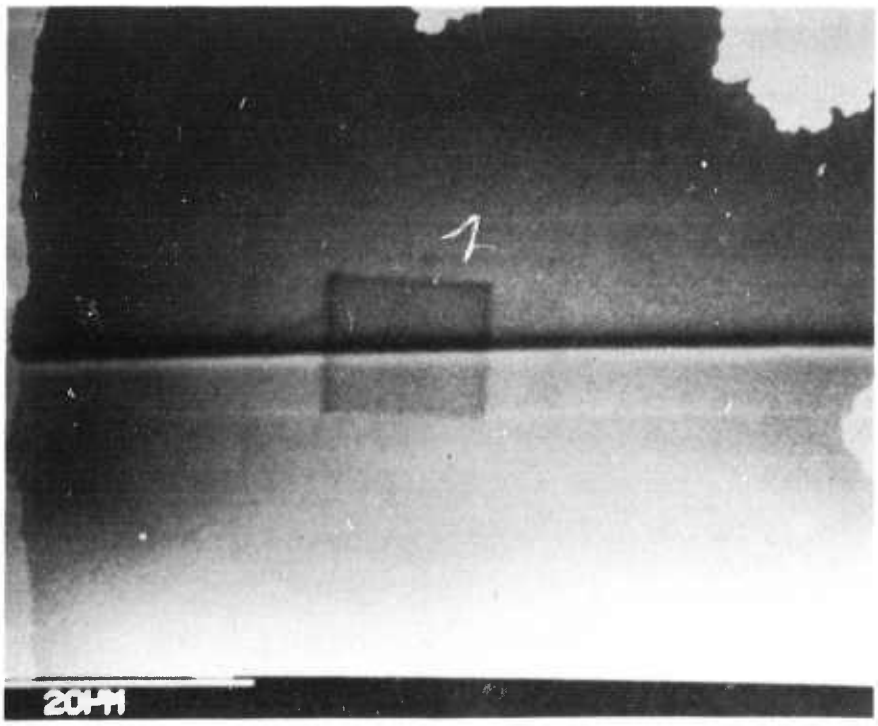


Figure 18 An SEM photograph of a 1 μm gate with a developed source image and a 60 nm overlayer of gold.

Figure 19 SEM view of a source image from a 2 μm gate with a 60 nm gold overlayer. View is along the gate width and the light region one third of the way up from the bottom of the picture is the semi-insulating edge of the etched region.

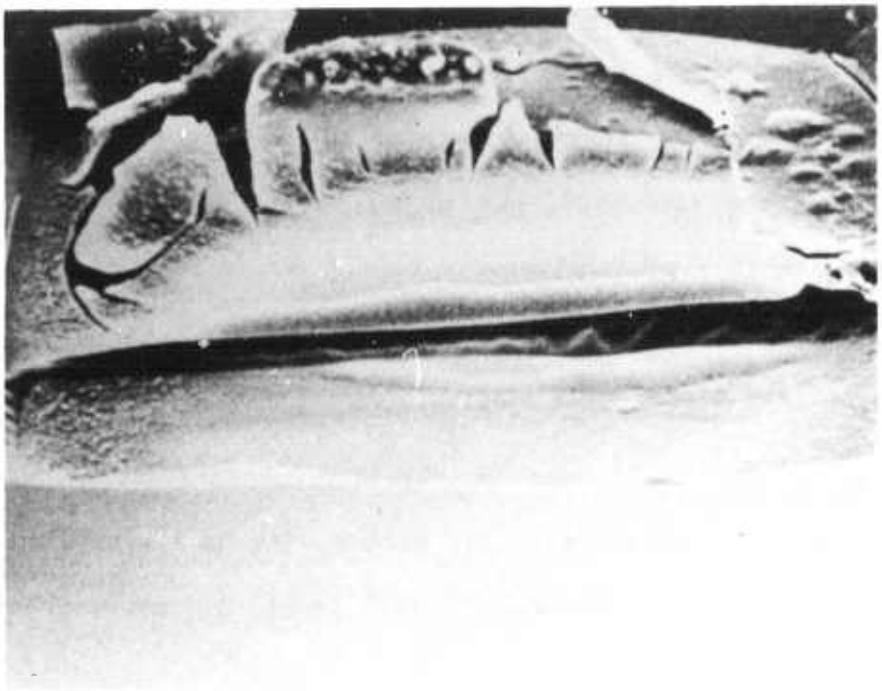


Figure 20 a)SEM photograph of a source image with a 160 nm overlayer of gold. Note that this 160 nm overlayer of gold is opaque.

electron beam; one can see the semi-insulating edge of the etched region about one third of the way up from the bottom of the picture. The next figure (Fig. 21) shows an enlarged view of the central portion of the membrane with the source image. Note that because of the angle between the direction of the incident electrons and the membrane no details within the source image can be seen in spite of the fact that the gate was 2 μm wide and the source image should be a few tenths of a micrometer less than that. Reorientation of the sample so that the incident direction of the electrons, the normal to the membrane and the viewing direction lie in a plane gives the view shown in Fig. 22. The gold that has been sputtered into the source image shows up as a bright line of the appropriate width.

Ideally one would want to obtain a cross-sectional view of the source image, but attempts to get such a view have thus far been unsuccessful because of the extreme flexibility of the membrane and the limited viewing angle at the bottom of the etched region. An alternative to obtaining a cross-sectional view was to utilize the transparency of these thin layers. Experiment had shown that 600 Å of gold was too transparent while 1600 Å of gold was nearly opaque. An intermediate thickness of the gold layer of 1200 Å revealed the contours shown in Fig. 23a and an enlargement is shown in Fig. 23b. The angles of incidence and viewing are adjusted so that a vertical projection of the gate, the source, the resist and the overlayer of gold can be seen. Some interpretation of the bands seen in Fig. 23b is needed and this is aided by the cross-sectional view of the structure shown in Fig. 24. This scaled cross-sectional view shows the known gate width of 1 μm, the

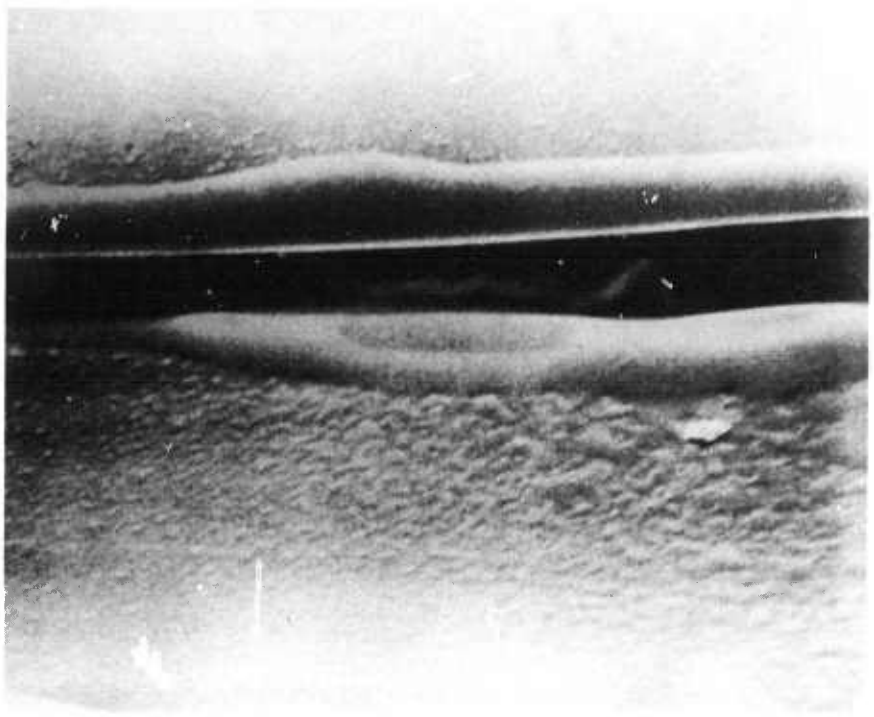


Figure 21 An enlarged view of the central portion of Fig. 20 containing the source image.

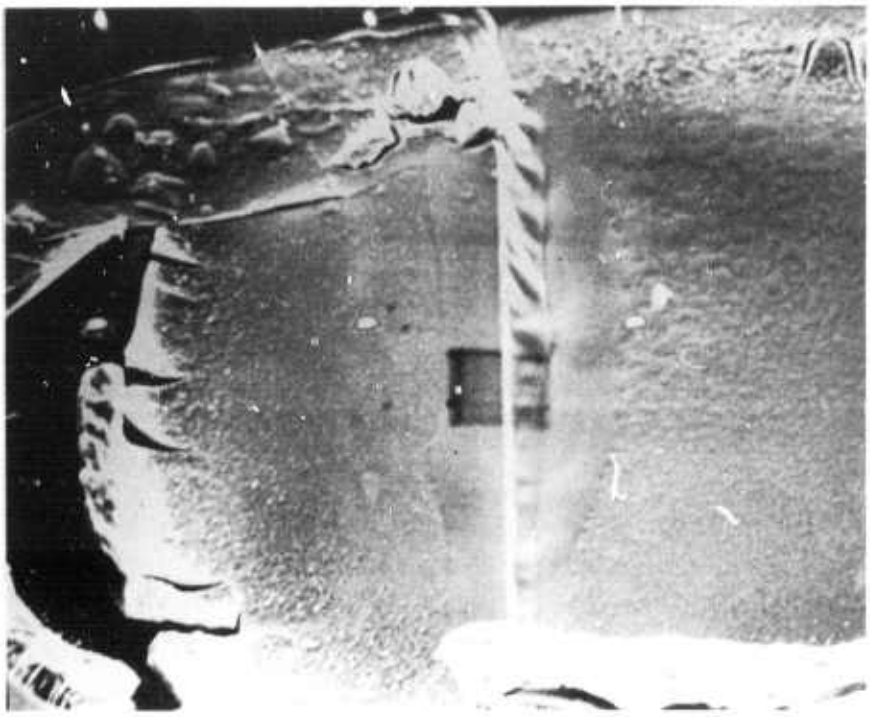
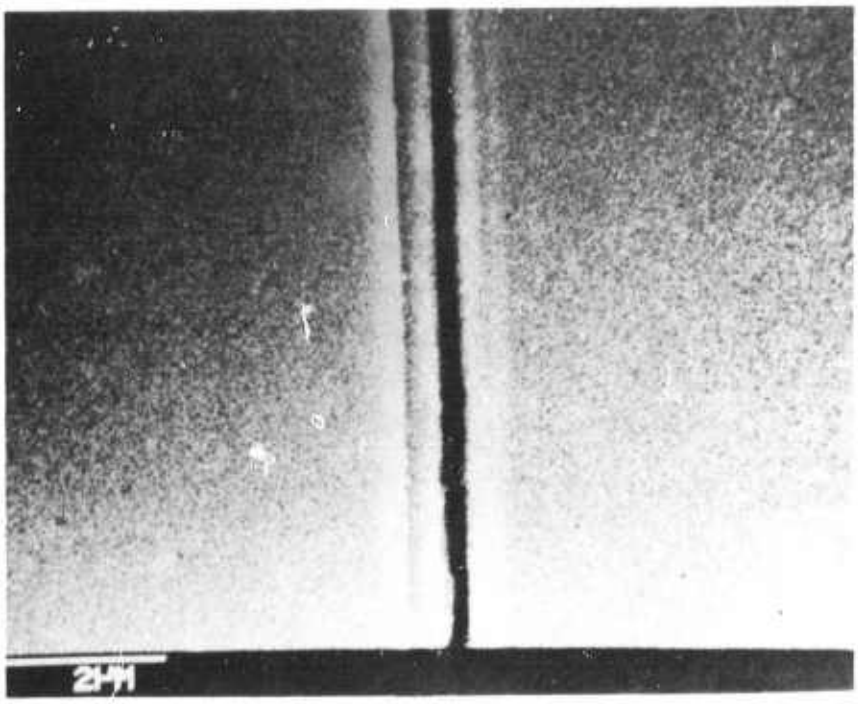
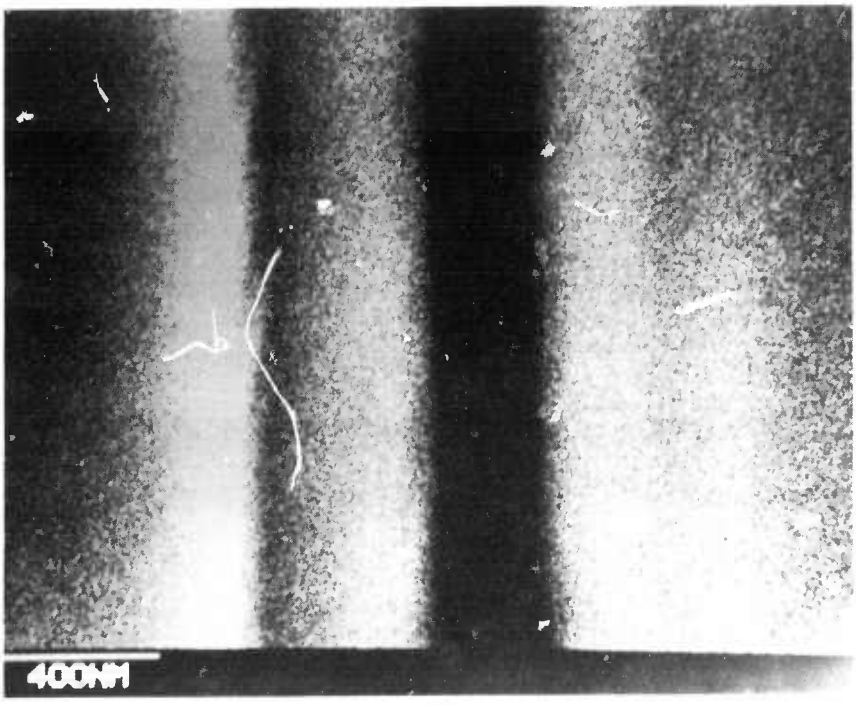


Figure 22 SEM view along the width of the source showing a bright source image with 160 nm overlayer of gold.



a)



b)

Figure 23 a)SEM photograph of source image with an intermediate 120 nm overlayer of gold. Being partially transparent the underlying resist and gate electrode are visible (see text for explanation); b)magnified view of a).

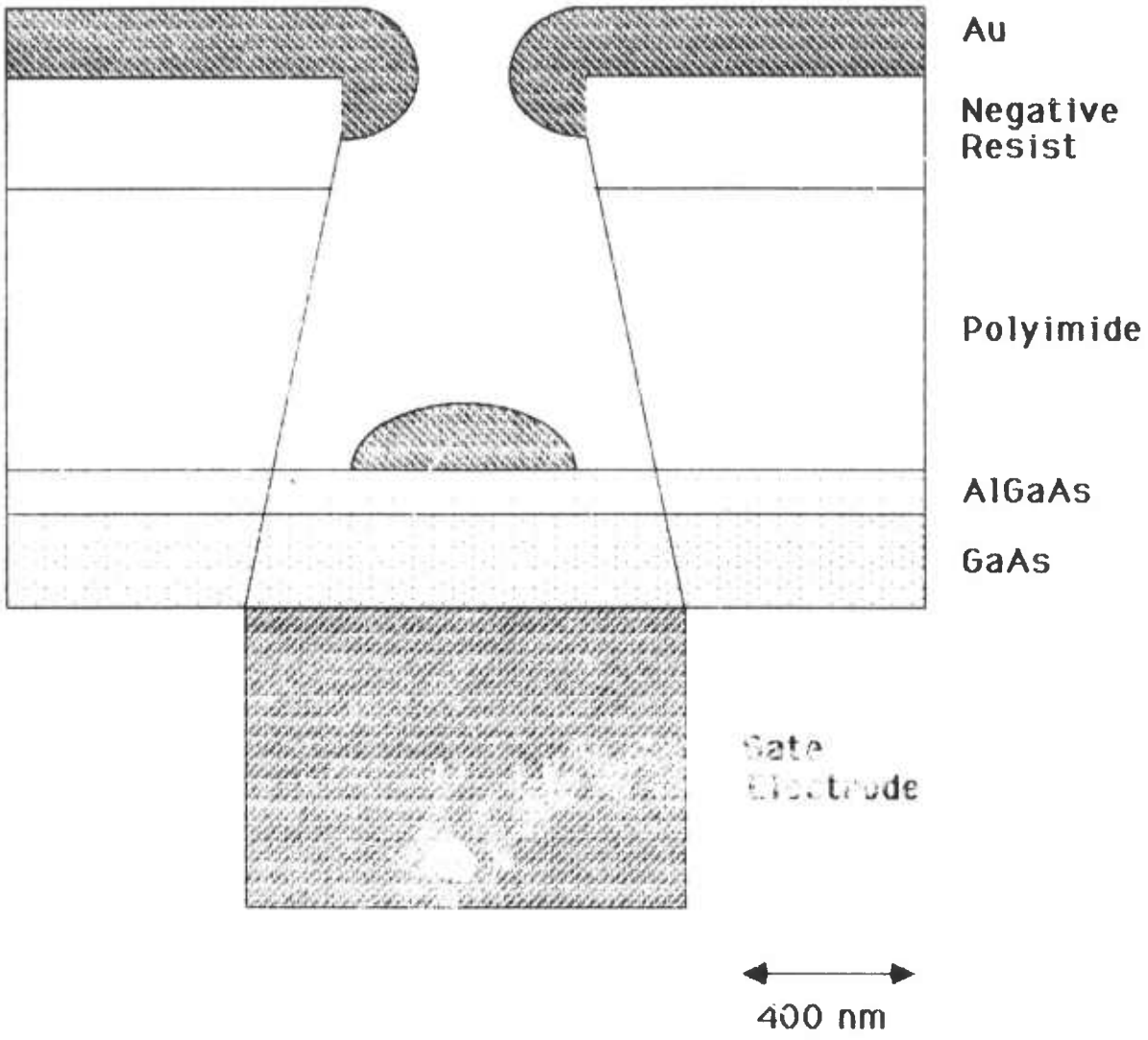


Figure 24 Schematic view of the cross section of the image in Fig. 23 drawn to scale.

active GaAs layer of 200 nm, the etch stop layer of 100 nm, a 700 nm layer of polyimide, a 300 nm layer of negative resist, and finally the 120 nm layer of gold.

Comparing Figs. 23b and 24 we identify the outermost bright bands with electrons that are backscattered from the gate electrode. The central dark band is the source opening which has been partially closed by the gold overlayer. These two associations allow us to estimate the narrowing of the source image produced by the lateral scattering of the electrons in passing through these multiple layers; this is shown by the two diagonal lines. Figure 24 shows that the source contact is approximately half the width of the gate contact and the question arises as to whether a finer geometry is possible. First we observe that the width of the gate and the source contacts could be halved by merely halving the thickness of the polyimide and removing the negative resist before evaporating the contact metalization. Second we note that the angle of overhang of the resist is a function of the exposure; a reduction in the exposure used in the example of Fig. 23b would result in less overhang (i.e. a longer source image. This exposure dependence of the overhang is a result of the high contrast of the resist. A further refinement of the contact geometry can, of course, be obtained by using higher energy electrons, but it appears that 30 kV electrons will be sufficient for mm-wave transistors at 90 GHz.

The correlation of the bands in Fig. 23 with the structure of Fig.24 convinced us that a usable source image had been made and for reasons of greater yield and shortened processing time a shift was made to UV processing. Our initial view of the UV processing was that the

diffraction effects would not permit us to achieve the electrode resolution required for operation at 90 GHz, but the decreased processing time would permit us to demonstrate a working transistor. Subsequent processing runs, however, revealed that the resolution we could obtain for the source image was indeed sufficient for mm-wave operation. Figure 25 shows a source image in the Probimide resist with a 100 nm overlayer of gold. If we conservatively estimate that the length of the source contact is 200 nm greater than the opening in the photograph then we arrive at a source length of 280 nm. The gate length used to produce this source image was 700 nm and recalling that the effective gate length in the OGST is approximately half the difference between the gate and source lengths we estimate the effective gate length to be 210 nm. This result indicates that UV lithography can be utilized to great advantage in fabricating mm-wave OGST's.

2.1.3.2 Source and Drain Fabrication and OGST Current-Voltage Characteristics

With the results of the experiments shown in Figs. 23 and 24 we proceeded with the transistor fabrication. With the intent of alloying to the active layer the AlGaAs stop layer was removed in an 80 °C solution of hydrofluoric acid [10]. Figure 26 shows an etched membrane with the Al GaAs layer partially removed. Then a layer of Probimide is spun onto the membrane, cured and a negative image of the source electrode is exposed and developed. Next a 100 nm layer of gold-germanium was evaporated and given a short alloying cycle to form the ohmic contact. The alloying cycle bakes the sample for a few seconds below the eutectic

Figure 25 SEM photograph of the smallest source image made with UV lithography, demonstrating the feasibility of fabricating a quarter micron wide source electrode with UV radiation of 436 nm.

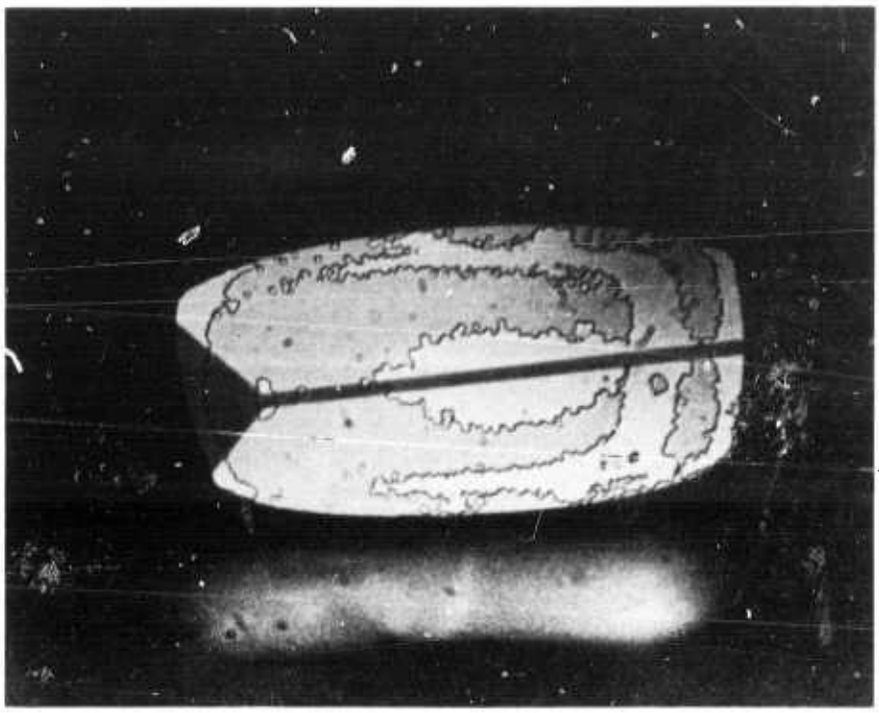


Figure 26 Partial removal of the AlGaAs stop-layer after immersion in an 80 °C solution of Hydrofluoric acid.

temperature to remove water vapor, then it is held for another short period at the eutectic temperature to improve the surface wetting and then the temperature is raised to 450 °C for about 30 sec to complete the alloying cycle. Figure 27 shows the alloyed layer of gold-germanium on the membrane; the bright line running vertically down the center of the membrane is the source image where electrical contact is made to the active layer.

After the source contact was alloyed another half micron of gold was evaporated to contact the line source contact and to strengthen the membrane. Thicker ground plane metallizations would be more conveniently formed by plating. The wafer containing the membranes is then removed from the sapphire substrate and remounted with the gate electrodes on top. At this point an isolation mask is put on the top surface and the active layer is etched away between the transistors to insure that individual transistor electrical charateristics are observed. The drain contacts are then made by conventional contact lithography, metallization and liftoff. Projection printing of the drain contacts would be preferable since occasionally a number of membranes are lost in the contact printing. The drain contacts are annealed with a temperature cycle similar to that used for the source. Figure 28 shows an optical micrograph of a completed OGST and Fig. 29 shows the I-V charateristic the gate-source Schottky contact.

An enlarged view of the gate and drain electrodes of an OGST are shown in transmitted light in Fig. 30. The transistor electrodes have been made transparent by limiting the thickness of the gold-germanium metallizations to about 600 Å. The segregation in this contact can be

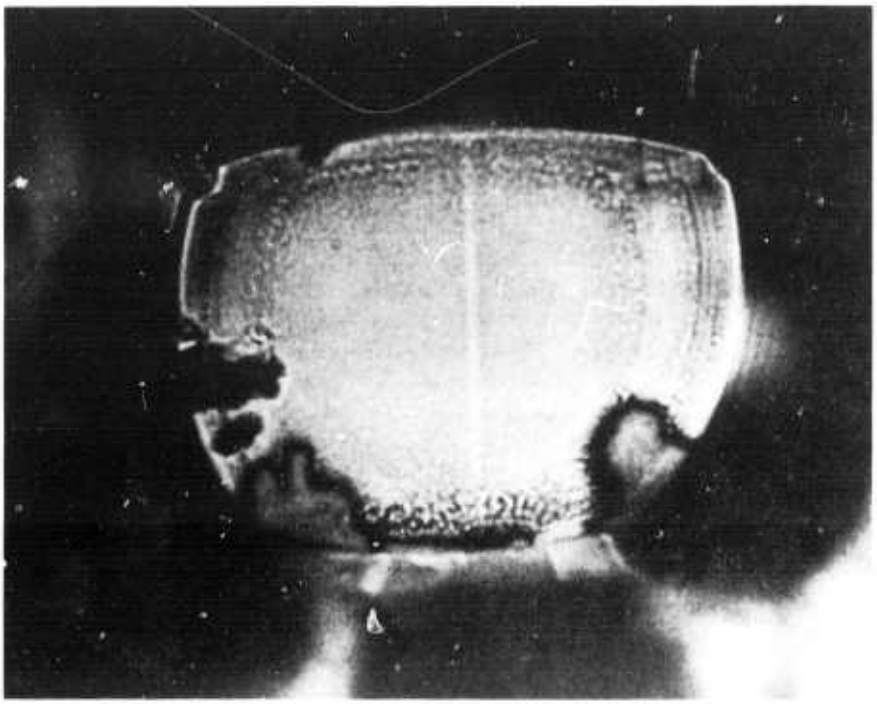


Figure 27 Alloyed source contact viewed from the source side; after a short soak at the eutectice temperature the temperature is raised to 450 °C for 30 sec.

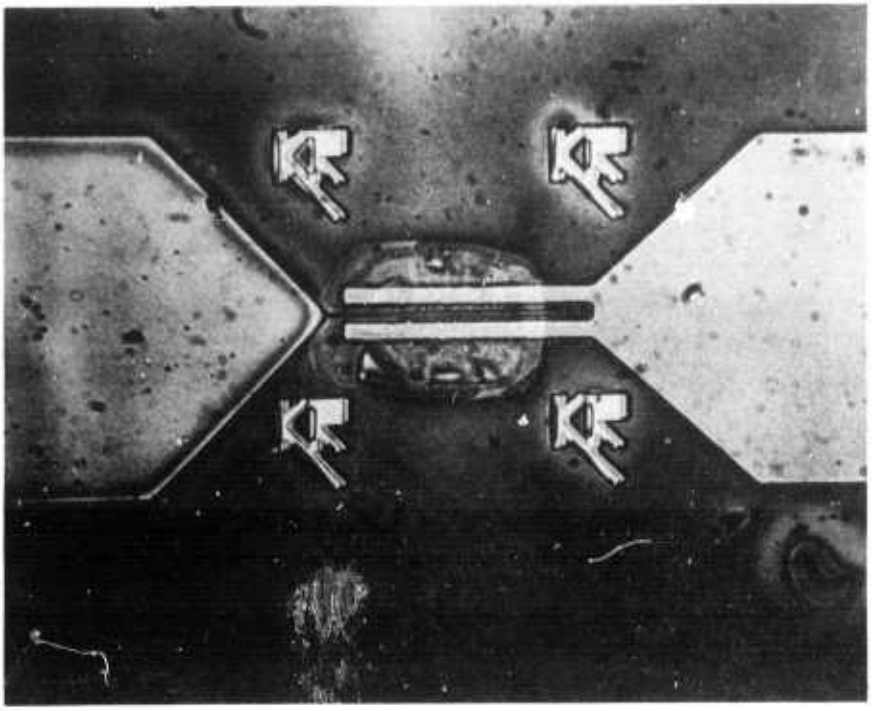


Figure 28 Optical micrograph of OGST from active layer side.

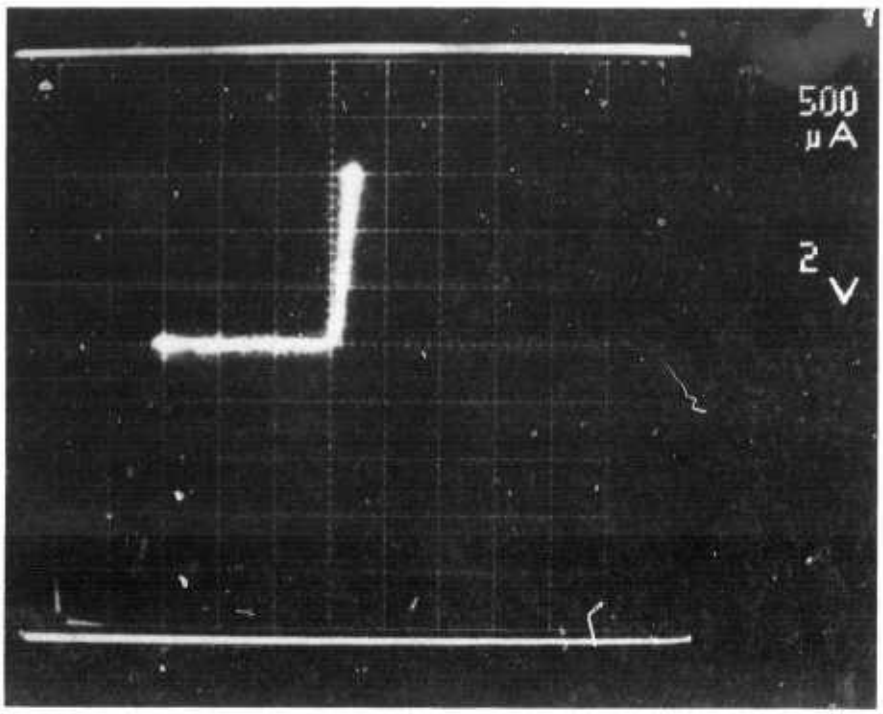


Figure 29 Gate-source I-V charateristic of completed transistor.

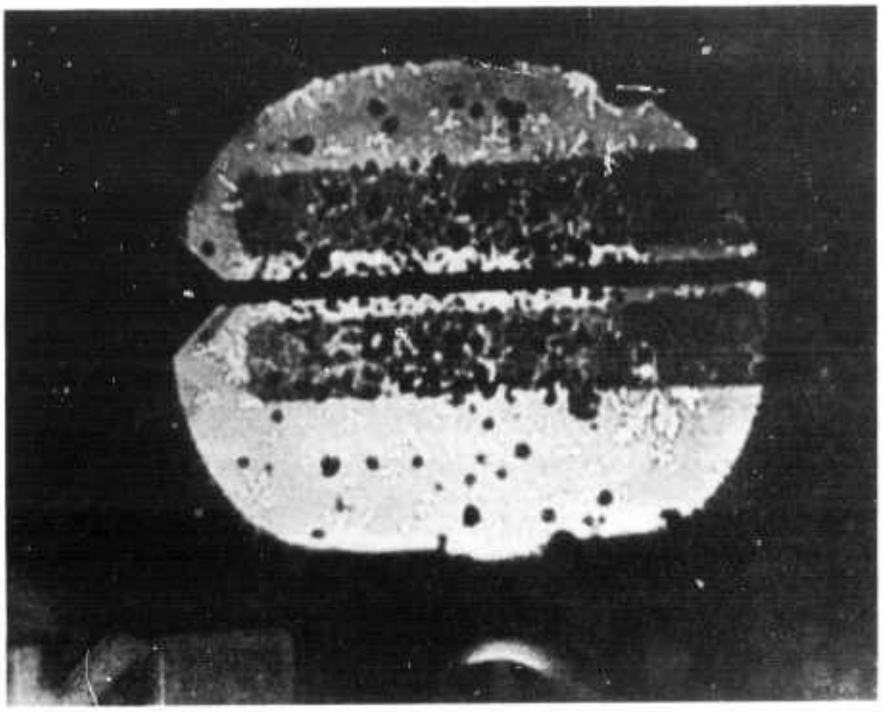


Figure 30 Optical micrograph of OGST with transparent electrodes in transmitted light; the Au-Ge contact layer was limited to 600 Å.

viewed quite graphically and supports the conclusion that a finer grained ohmic contact for the source would be an improvement.

Completed transistors were mounted in a probe station for the evaluation of the electric characteristics. Figure 31 shows the drain current vs the drain voltage as a function of the gate voltage when the probes were not terminated. The instabilities indicate that oscillations were occurring and that there was at least some radio frequency gain in the transistor. When the probes were terminated in wide band 50 Ω loads the transistor characteristics shown in Fig. 32 were obtained. The transconductance indicated by the data in Fig. 32 is only some 50 μS, which is probably attributable to a poor source contact. The data of Fig. 31, however, indicate a transconductance of 1.2 mS; there is still room for much improvement in the contacts.

Having shown the feasibility of constructing the OGST on a 200 nm membrane of GaAs we reconsidered the subject of the transmission line design. During the transistor processing it was advantageous to limit the area of the thin membrane to some 80 x 100 μm for reasons of strength against the stresses of processing. After completion of the processing it was considered that the supporting substrate surrounding the membrane might be removed to facilitate embedding the transistor in an external transmission line. A simpler solution to the problem was found and the resulting design is shown in the micrograph of Fig. 33. The half micron gate shown in the figure has a characteristic impedance of about 15 or 16 Ω. As the gate electrode leaves the membrane the electrode is widened over the region of the etched depression on the other side of the wafer. At the edge of the etched region where the

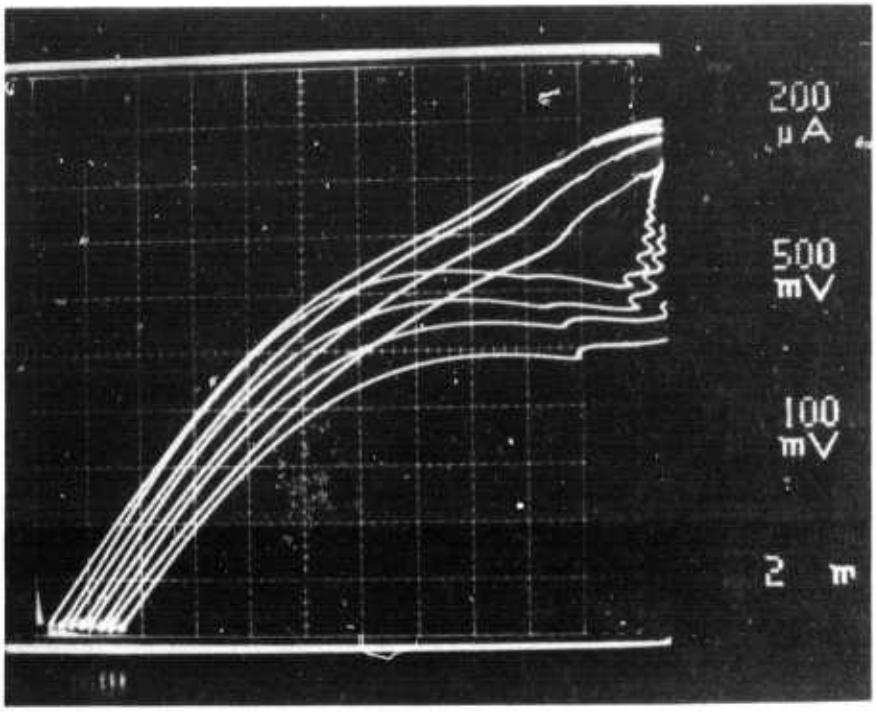


Figure 31 Unstable I_D vs V_D as a function of V_G without probes being terminated with 50 Ω.

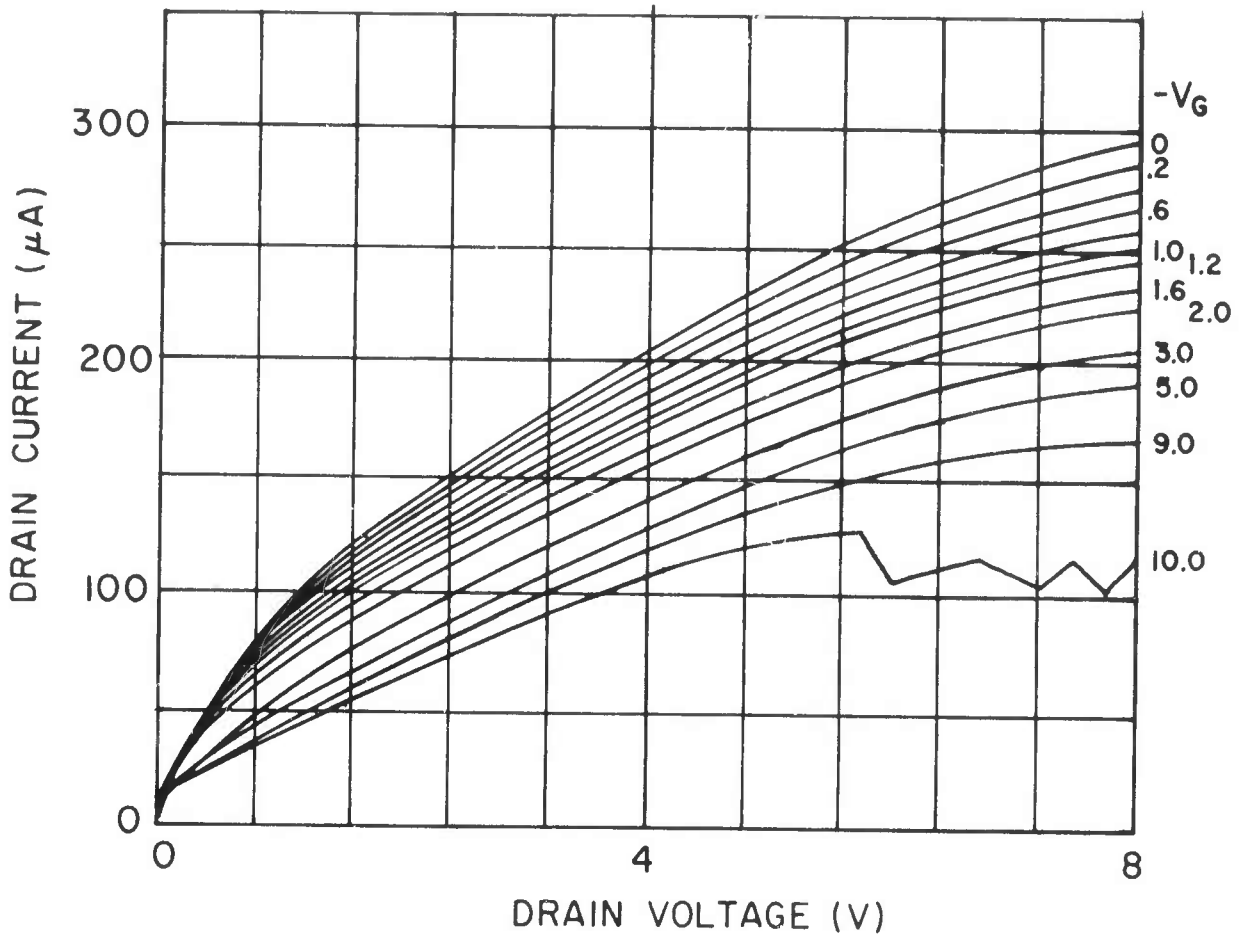


Figure 32 Stabilized I_D vs V_D as a function of V_G with probes terminated with 50 Ω.

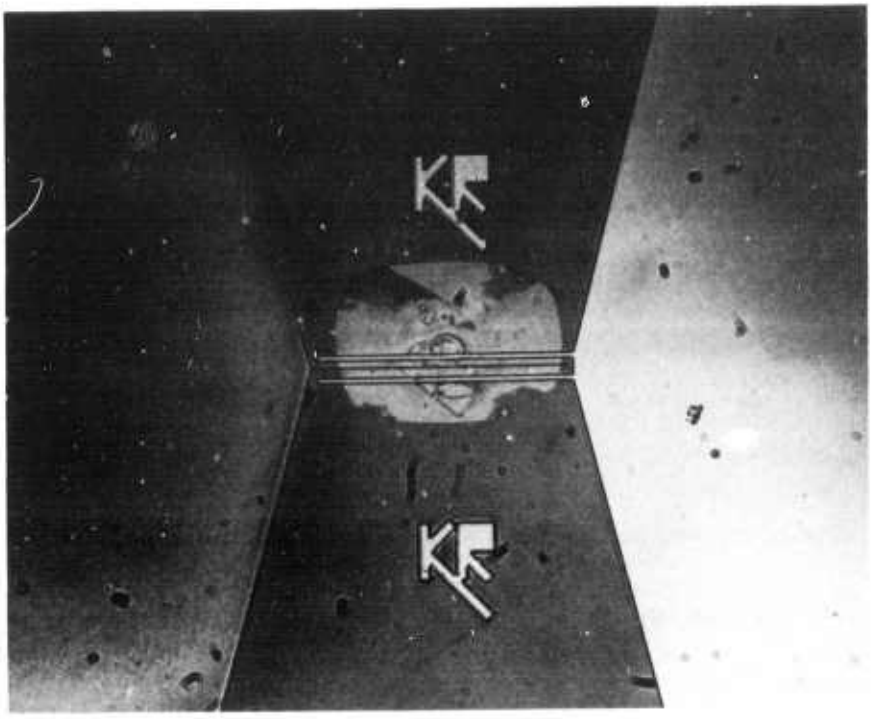


Figure 33 Photograph of constant characteristic impedance design including the gate and drain electrodes.

substrate is 75 μm in thickness the width of the gate electrode becomes constant at a value corresponding to a characteristic impedance of 15 Ω. In a similar fashion the drain lines with a dielectric comprised of the active layer and a layer of Probimide are of a length corresponding to a characteristic impedance of 15 Ω. The drain line also widens as it comes off the membrane to accomodate the change in the substrate thickness and maintain a characteristic impedance of 15 Ω. Thus this transistor design maintains a constant transmission line impedance from the submicron gate electrode to a substrate transmission line that is of sufficiently large dimension that it can be embedded in an external microstrip transmission line. The embedding of the transistor in a microstrip line will be described in Section 2.3.4.

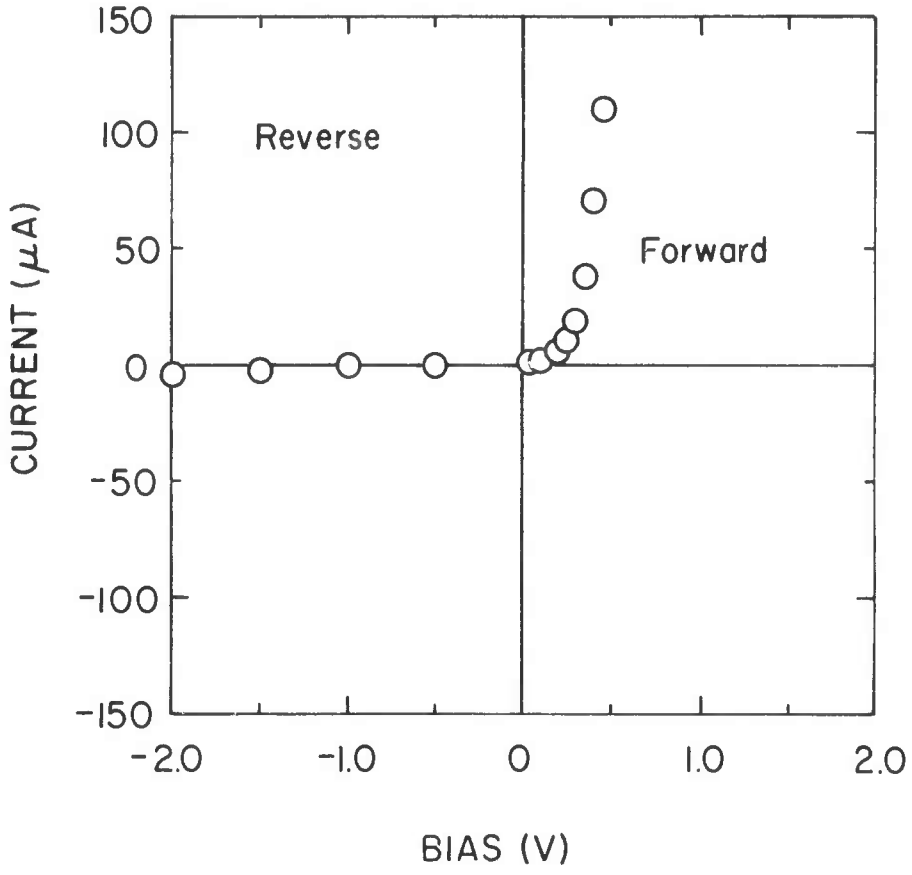
2.1.4 Molybdenum-Germanide Ohmic Contacts (K. Rauschenbach, C. A. Lee)

There are two ohmic contacts that have to be made in the OGST, the drain contact and the source contact. The easiest of these is the drain contact where the metallization can be alloyed to an n+ implanted area on either side of the gate. A conventional gold-germanium alloy will make an acceptable contact [2]. The source contact in the OGST, however, presents some additional restrictions. If this contact is an alloyed contact then a high degree of uniformity of the wetting and a low degree of segregation must be achieved for it to be a satisfactory one. The source contact must be made directly on the 200 nm active layer.

The ideal solution for a good source contact is to selectively grow an n+ layer in the source opening and then make a conventional alloy

contact to the n+ layer. Although this solution has been shown to be feasible in the fabrication of the permeable base transistor, it is beyond the capability of our facilities. Instead we have concentrated our attention on achieving good wetting with gold-germanium alloys and have explored sintered ohmic contacts such as the molybdenum-germanium contact described by Tiwari et al [1]. Very uniform wetting has been obtained by sputtering the alloy coating onto a heated substrate with an appropriate bias. This procedure removes the oxide while the bias potential is kept sufficiently low that ion damage is avoided. To demonstrate this alloying procedure a thin film silicon diode was fabricated [11]. A 50 μm diameter Schottky contact was made on one side of a 150 nm thick silicon membrane. The other side of the membrane was completely covered with an alloyed contact of gold and antimony. Capacitance measurements verified that the depth of the alloying was less than 50nm. Figure 34 shows the current-voltage characteristic of the diode. An alternative procedure to obtain more uniform wetting was to employ pulse heating. Pulse heating has the advantage that with GaAs surface damage is much less.

Sintering and diffusion of impurities, as is the case with the molybdenum-germanium contact, is a promising technique for a high degree of control over the penetration of the contact. The description of this contact given by Tiwari et al [1] seemed to indicate that the film was composed mainly of $Mo_{13}Ge_{23}$ after annealing at 745 °C. They also argued that dominance of the Mo-Ge interaction caused arsenic to play an insignificant role in the film. To test this hypothesis we sputtered and annealed Mo-Ge films onto silicon dioxide and onto semi-insulating GaAs.



Silicon Schottky diode on a 1500 Å membrane.

Figure 34 Current-voltage characteristic of a diode made on a 150 nm silicon membrane; a 2 mil diameter platinum Schottky contact is made on one side of the membrane and a broad area alloyed gold contact is made on the other side to illustrate the uniformity of wetting and the controlled penetration of the contact that can be achieved.

The sheet resistance of the contact on the silicon dioxide was 500 Ω/□ while the sheet resistance of the film of the GaAs was only 24 Ω/□. We concluded, therefore, that either arsenic or gallium played a significant role in the conductivity of the film. To further verify this conclusion a SIMS analysis was carried out on annealed and unannealed Mo-Ge films in collaboration with Prof. G. Morrison and W. Ausherer of the Cornell Chemistry Department.

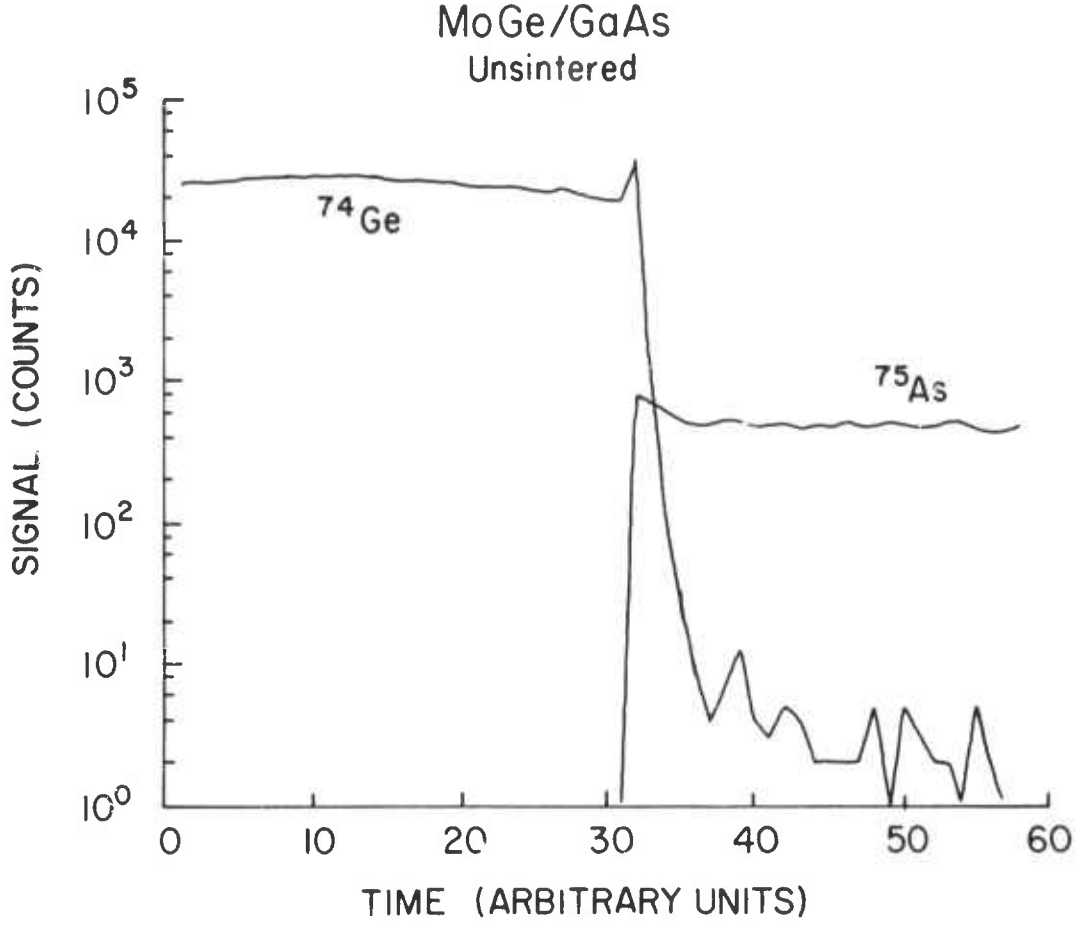
The SIMS analysis turned out to be more complicated than anticipated because of mass interferences (e.g. ^{74}GeH and ^{75}As). The distributions of germanium and arsenic for unsintered and sintered films on GaAs with a tungsten overlayer are shown in Figs. 35 and 36. The germanium diffuses nicely into the GaAs substrate beyond the interface as does the arsenic into the contact. In fact, sufficient arsenic penetrates the contact to account for the alteration in its conductivity. The molybdenum penetration upon sintering is slightly slower than that of the germanium as is the gallium from the GaAs into the contact. These profiles are in agreement with those of Tiwari et al and are consistent with the low contact resistances they reported. The contact resistance we have measured, however, are still about a factor of ten higher than their values.

2.2 DEVICE DESIGN, SIMULATION, and ANALYSIS

2.2.1 Process Simulations for Dual Surface Lithographies

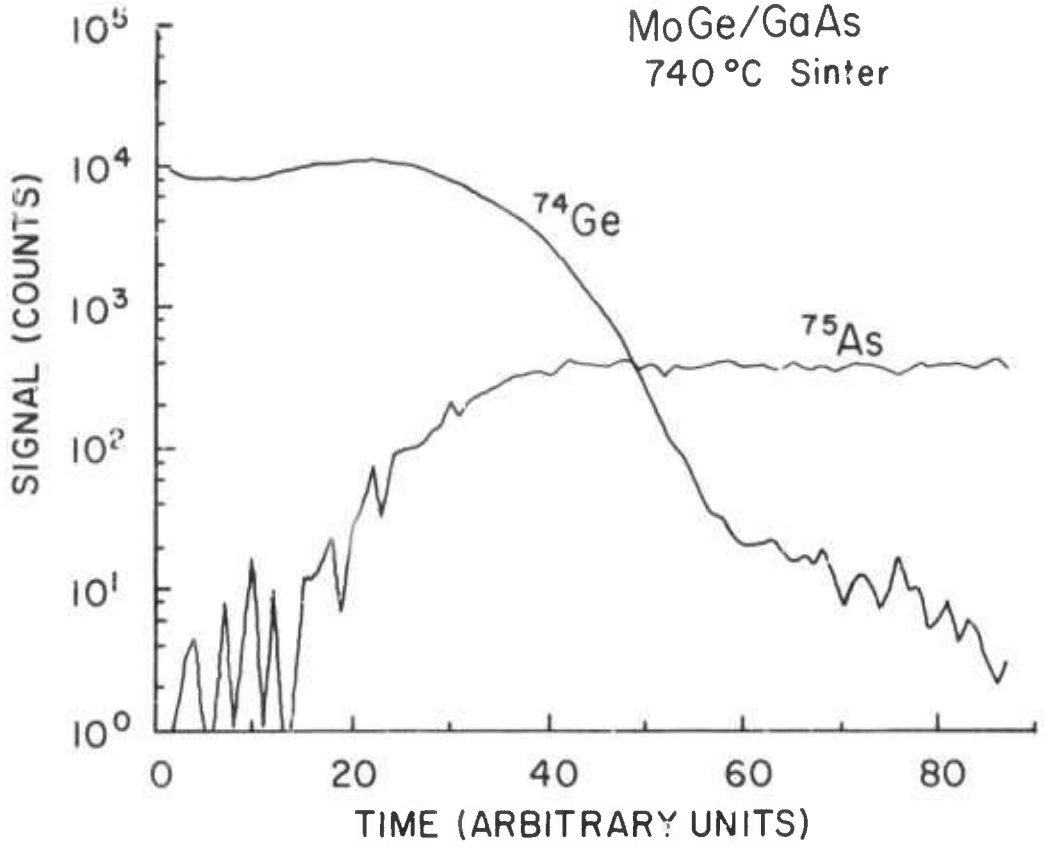
(J.P. Krusius, A. Perera)

2.2.1.1 Introduction



Traces corrected for ^{74}GeH-^{75}As interference.

Figure 35 SIMS profile of arsenic and germanium in a molybdenum-germanium contact before sintering. The traces have been corrected for mass interference of ^{74}GeH and ^{75}As. The thickness of the contact is 100 nm.



Traces corrected for ^{74}GeH - ^{75}As interference.

Figure 36 SIMS profile of the molybdenum-germanium contact shown in the previous Fig. 35 after sintering at 740 °C; the depth scale (arbitrary units) is the same.

Dual surface lithography is here defined to mean aligned sequential or simultaneous lithography on two opposite surface of a substrate. Aligned is clearly a key word is this definition. If no alignment requirements have to be met, the patterns on the two surfaces are completely independent and can be defined using single surface lithography on both surfaces.

The novel dual surface self-alignment concepts developed in this work are based on the integration of the exposure mask into the substrate structure and subsequent exposure of the backside resist through the substrate. The substrate resides thus between the mask and the resist. The exposure can in principle be done with photons, electrons, ions, and x-rays. The transmission characteristics of the substrate will limit the materials choices and the thickness of it. If the substrate is thin compared to the minimum feature size, one expects to have a faithfull replication of the mask image in the resist as in conventional contact printing. For thicker substrates and narrower lines edge lateral effects will be important and result generally in a reduced resist line width compared to the mask features. In some cases, such as the OGST device, this may be a desired feature, while in others inside or outside spacer techniques can be used to adjust the final linewidth after pattern transfer.

In the following self-aligned dual surface lithography with electrons, ions, and x-rays will be explored in closer detail. Optical photons have not been considered, since semiconductor type substrates are of primary interest. Most semiconductors have an absorption coefficient of the order of 1. 10^6 cm^{-1} for photon energies higher than 3 eV, and

would thus even for a 1000 A membrane show an intensity reduction of 5. 10^{-5}, which is quite impractical. Further, submicron lines are desired here and hence optical photons are undesirable also from the point of view of diffraction.

2.2.1.2 Self-Aligned Dual Surface Electron Beam Lithography

Electron beam exposure of a backside resist through a semiconductor substrate requires that the range of electrons should be comparable to the combined thickness of the substrate and resist structure. For electron energies typically used in microfabrication, i.e. 100 keV or less, this limits the combined thickness to less than 1 μm. This is still more than is needed for membrane type semiconductor structures, such as the OGST device.

The exposure characteristics with electrons have been explored theoretically using the Monte Carlo simulation method [12]. It allows to simulate the trajectories of individual electrons travelling through the multi-layer mask/substrate/resist structure and accumulate the total deposited energy distribution. The latter can be used to predict the developed image profile in the resist. For simplicity it is assumed that the mask lines on the top side of the substrate are non-transparent to electrons, and that the mask line edges are perfectly vertical. Both assumptions can be satisfied for practical conditions as is shown in Sec. 2.1.2. As a consequence of these two assumptions the Monte Carlo simulations can be performed for a point entrance in the unmasked region. Mask effects can accurately be modeled by convoluting the point entrance results with the mask profile. The Monte Carlo program EXPOL

[13] has been used for all electron simulations. No secondary electrons are tracked by EXPOL. Their effect will be discussed separately.

The following structure has been chosen for the discussion of the characteristics of the self-aligned dual surface electron beam lithography. A 500 nm thick silicon membrane serves as the substrate. The non-transparent mask lines are on the top surface. The high resolution positive tone resist PMMA with a thickness of 500 nm is used as the backside resist. The energy of the incident electrons has to be of the order of 35 keV or more in order to have most of them traverse through the substrate/resist structure. The simulated electron trajectories for a point entrance in the non-masked area for the incident energies of 35, 75, and 125 keV for 500 electrons are shown in Fig. 37. The trajectories lie within two concentric cones because of the large density ratio between the membrane and resist materials. The density of the backside resist is lower and hence the lower cone is wider. The exit width at the lower surface of the resist decreases rapidly with increasing energy. The characteristic exit width for 75 keV electrons is about 300 nm. The corresponding deposited energy distributions for 35, 75, and 125 keV for 100,000 electrons are given in Fig. 38. A cell size of 40 nm x 40 nm has been used. The deposited energy distributions are considerably narrower than the trajectory diagrams indicate, since the latter do not resolve the center region of the trajectory cone well. The width of the energy distribution measured at the 10 per cent level from the maximum is now only 300, 110, and 70 nm for 35, 75, and 125 keV respectively. The lateral tail of the energy distribution is wider than its center part, but this should not have much significance because of the

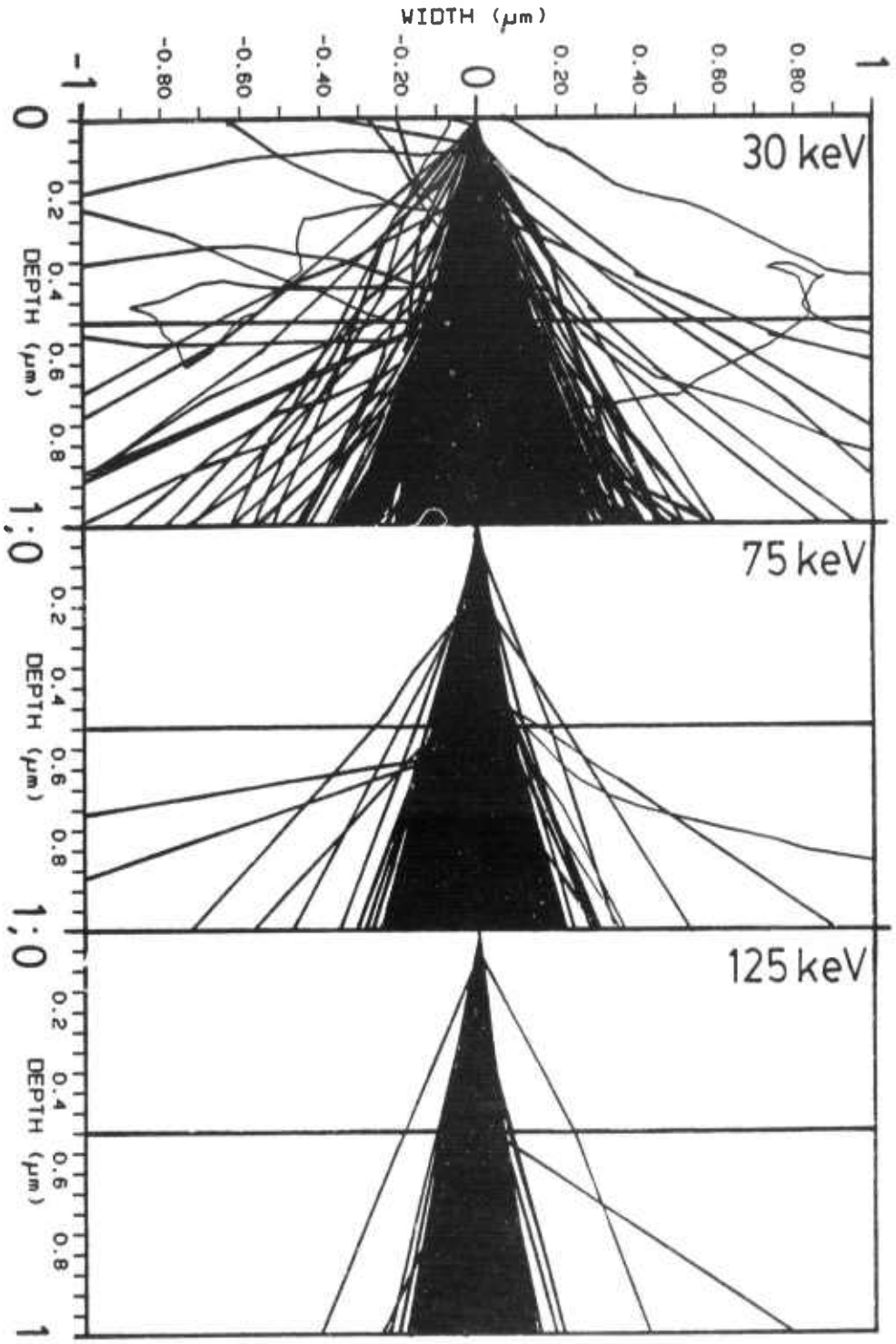


Figure 37 Electron trajectories for normal incidence, point entrance, and incident energy of 30, 75, and 125 keV (top, middle and bottom panels respectively). A 2 μm x 1 μm cross section with 500 nm Si (top) and 500 nm PMMA (bottom) is shown in each panel.

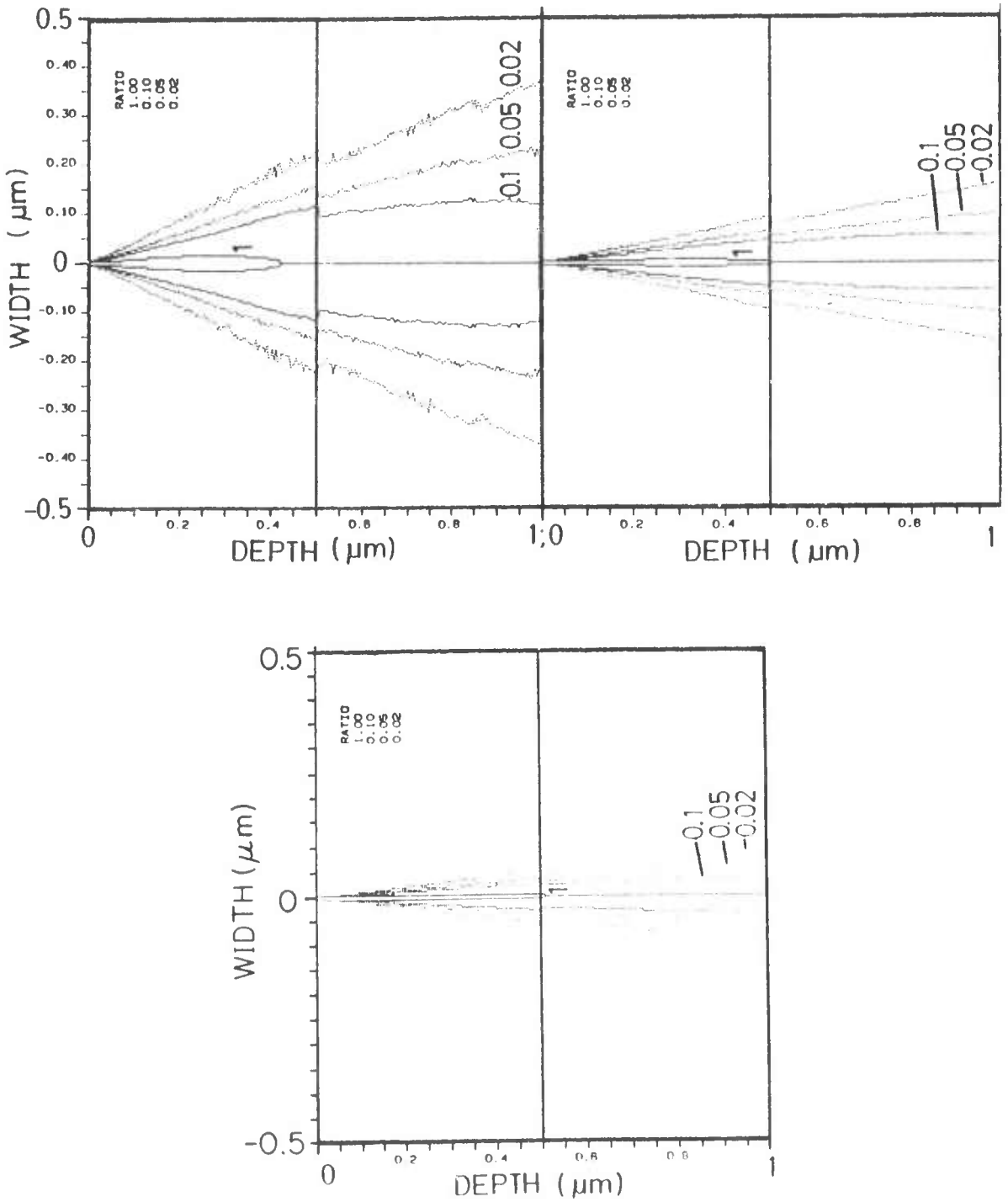


Figure 38. Deposited energy distribution for normal incidence, point entrance, and incident energy of30, 75, and 125 keV (top, middle, and bottom panels respectively). A 1 μm x 1 μm cross section with 500 nm Si (top) and 500 nm PMMA (bottom) is shown in each panel. The energy contours have been normalized with respect to the threshold energy such that the relative contour 0.1 corresponds to 1.0 10^{22} eV/cm^3.

low energy levels. While the inclusion of secondary electrons would introduce a number of electrons traveling predominantly normal to the direction of incidence, their mean lateral path length is not larger than 5 nm [12]. Thus their effect on the broadening of the present energy distributions is quite small.

The energy distributions for the masked exposure can be readily obtained via convolution with the mask profile. Convolution has been performed using the above cell size of 40 A. Fig. 39 shows the final masked energy distribution for 600 and 300 nm wide mask lines for an incident energy of 75 keV. Outside the mask lines the resist receives the full exposure dose. The deposited energy density falls to half of its value in the first 50 nm and to a quarter in 120 nm from the mask edge measured along the lower surface of the resist. The width of the resist area that receives an exposure energy of less than half of the unmasked area, is for the 300 nm wide mask line still 180 nm wide, if measured along the lower surface of the resist. For the 300 nm wide mask line the energy distributions from both edges merge for lower contours in the lower half of 500 nm thick resist layer.

To first order the development of the resist image can be modeled by a single threshold energy. This neglects any non-linearity in the resist development. For PMMA a good value for it is $E_T = 1.\ 10^{22}$ eV/cm^3 for a line dose of 100 nC/cm [12]. Based on this the mask line widths of 600 and 300 nm result in resist line widths of 510 nm and 180 nm for a 500 nm thick resist, and widchs of 540 nm and 230 nm for a 250 nm thick resist, again measured at the lower surface of the resist. Better development models [14-16] would result in a somewhat narrower developed

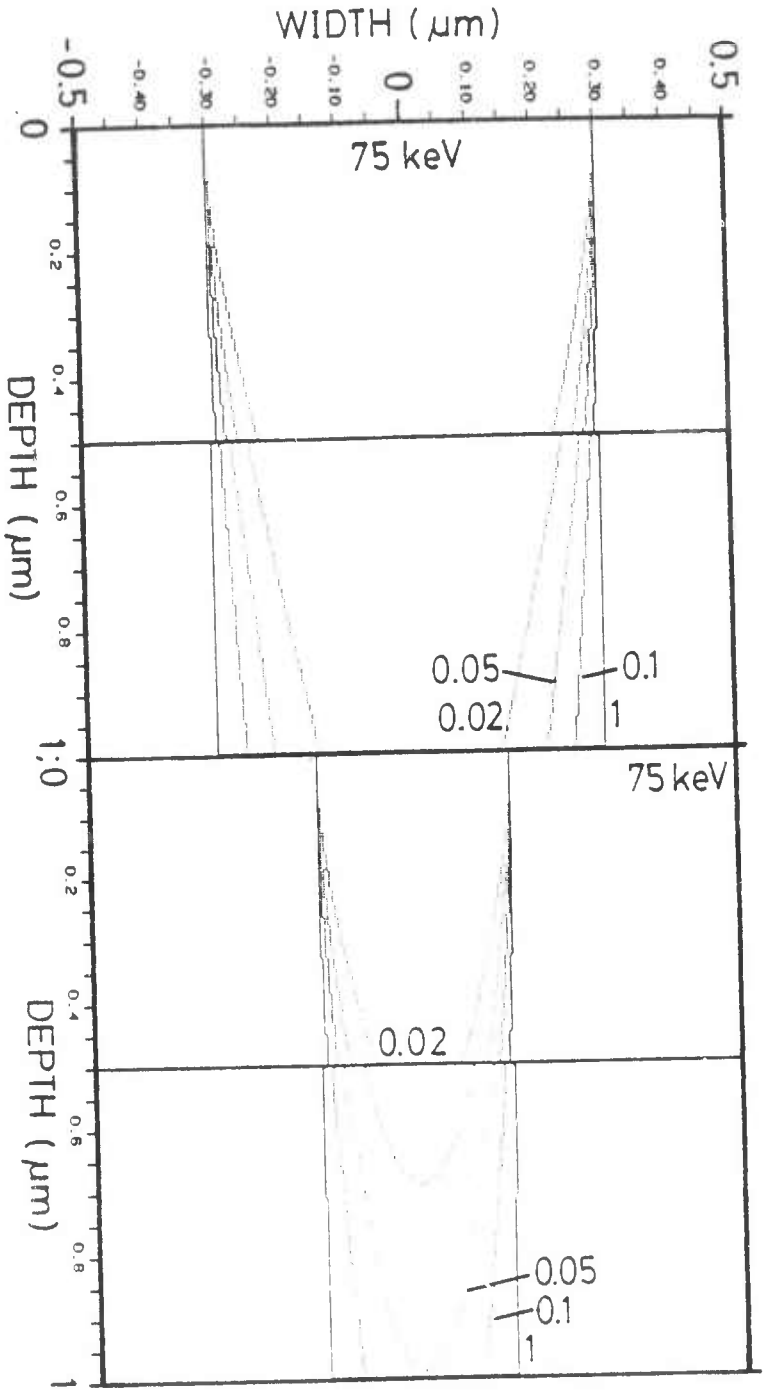


Figure 39 Deposited energy distribution for masked electron exposure for 75 keV incident energy and mask width of 600 nm and 300 nm (top and bottom panels respectively). A 1 μm x 1 μm cross section with 500 nm Si and 500 nm PMMA is shown in each panel. The mask line is centered at 0.0 on the top surface.

resist line, since the etch rate goes with $[1+(E/E_0)]^2$, where E is the local deposited energy and E_0 a reference energy. A more accurate development model will, however, not change the main conclusions of this original study, and hence no attempt is made to predict a more quantitative width for the resist lines. The edge shape of the resist lines will be more vertical for higher incident energies and thinner resists, but will always show sloped edges.

The simulated 500 nm Si membrane corresponds roughly to a GaAs thickness of 220 nm, and thus the extrapolated edge loss for an OGST with a 0.5 μm long gate line and a 0.9 μm thick backside resist is of the order of 100 nm for 75 keV electrons, i.e. result in a source length of about 0.3 μm.

.sp 2 2.2.1.3 Self-Aligned Dual Surface Ion Beam Lithography

Self-aligned dual surface ion beam exposures proceed analogous to the electron beam case. Since ion ranges, because of their large radius and mass, are much smaller than that of electrons for the same energy, light ions with higher incident energies and thinner substrates have to be used. For this reason only protons have been explored here. The exposure characteristics for ions have also been explored theoretically using the Monte Carlo particle simulation method. Again the particle trajectories and the deposited energy distribution are simulated first for a point entrance, and then the mask is accounted for via convolution. The same assumptions about the characteristics of the mask are made. In order to compare the electron and ion exposure characteristics, both the thickness of the silicon membrane and the resist layer have been kept at 500 nm. The incident energies have been raised

correspondingly. The Monte Carlo program TRIM [17] has been used for all ion simulations.

The simulated proton trajectories for 125, 200, and 400 keV are given in Fig. 40 for 100 particles. The trajectories lie again within two concentric cones, which however are much narrower than those for electrons. The exit width of the trajectory cone is 330, 190, and 100 nm for the incident energies of 125, 200, and 400 keV respectively. The associated deposited energy distribution for 2500 particles and a cell size of 10 nm x 10 nm are shown in Figs. 41 and 42. The penetration depth of ions is seen to be drastically smaller than that of electrons. The ion energy of 400 keV is roughly comparable to 125 keV for electrons. For 400 keV protons the exit width, measured at the 10 per cent contour from the maximum, is now 61 nm. In the longitudinal direction along the line of incidence the energy distribution falls less rapidly. At the membrane/resist interface the energy distribution has fallen to 58 per cent from the maximum value at the entrance point, and at the lower surface of the 500 nm thick resist a value of 23 per cent is encountered. The convoluted energy distribution for the masked exposures are similar to those for electrons and will not be reproduced here. With the threshold energy of F_T=1. 10^{22} ev/cm^3 and a line dose of 30 pC/cm, the loss on line width per edge is now about 25 nm. Because of the heavier incident particle mass, it is expected that secondary electrons would have a longer average range than those generated during an electron beam exposure. Also, the resulting heavy energy and momentum deposition would be likely to introduce severe damage to the thin membrane, and thus self-aligned dual surface ion beam lithography seems the

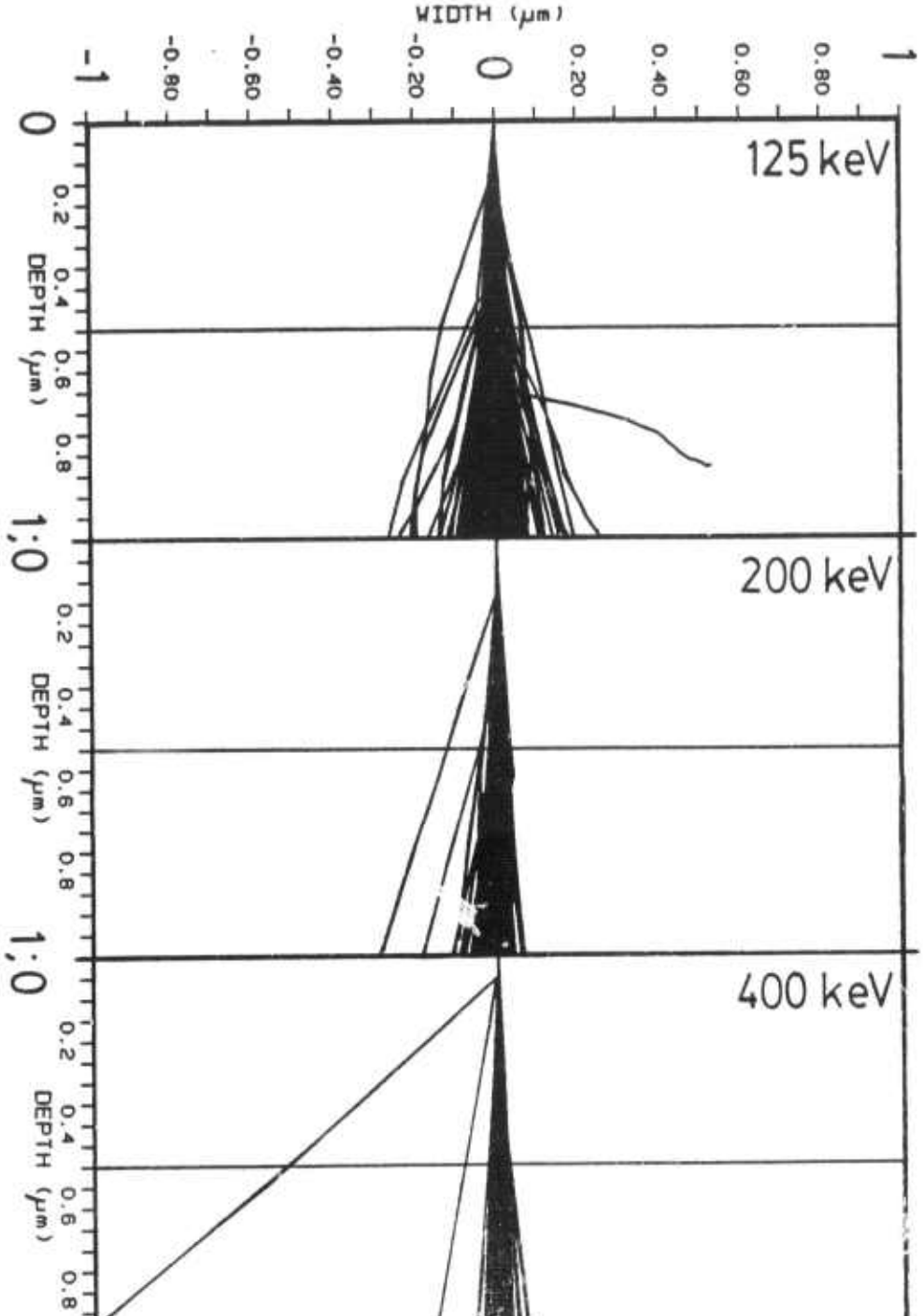


Figure 40 Proton trajectories for normal incidence, point entrance, and incident energy of 125, 200, and 400 keV (top, middle, and bottom panels respectively). A 1 μm x 2 μm cross section with 500 nm Si and 500 nm PMMA is shown in each panel.

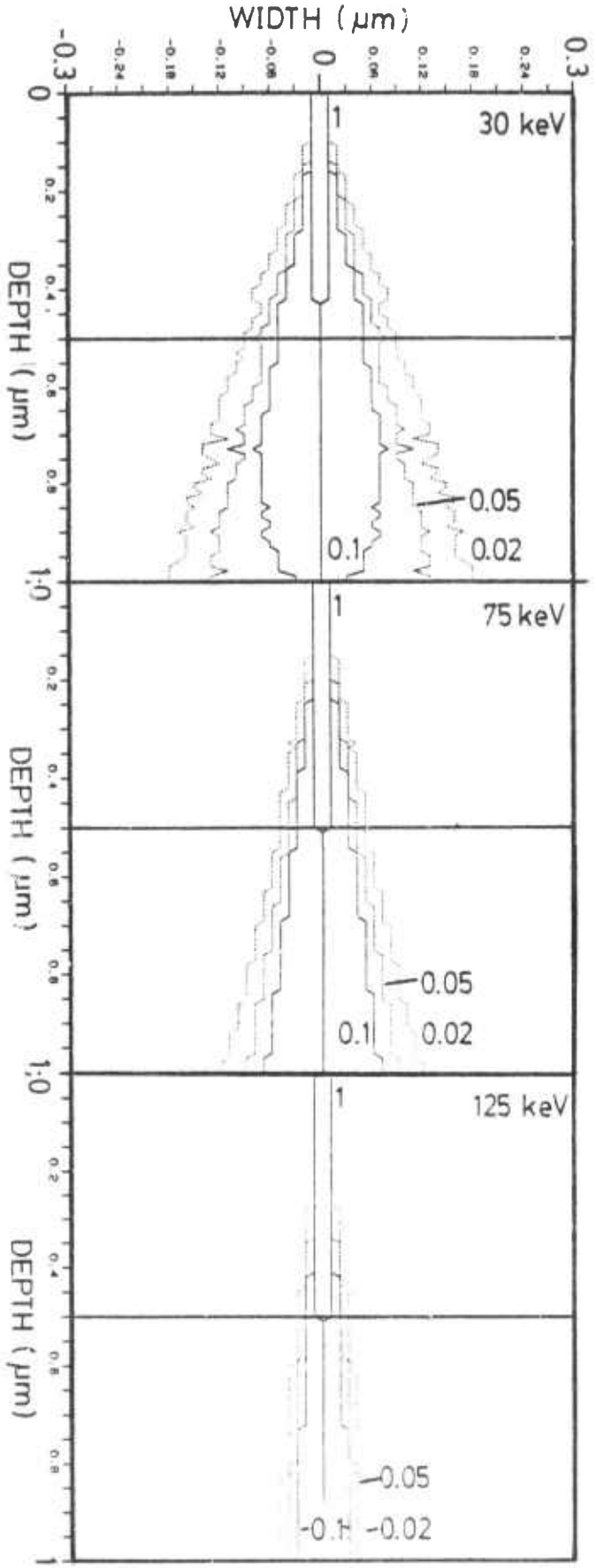


Figure 41 Deposited energy distribution for proton exposure for normal incidence, point entrance, and incident energy of 125, 200, and 400 keV (top, middle, and bottom panels respectively). A 0.6 μm x 1 μm cross section with 500 nm Si and 500 nm of PMMA is shown in each panel. The energy has been normalized with respect to the threshold energy such that the relative contour 0.1 corresponds to $1.0\ 10^{22}$ eV/cm^3.

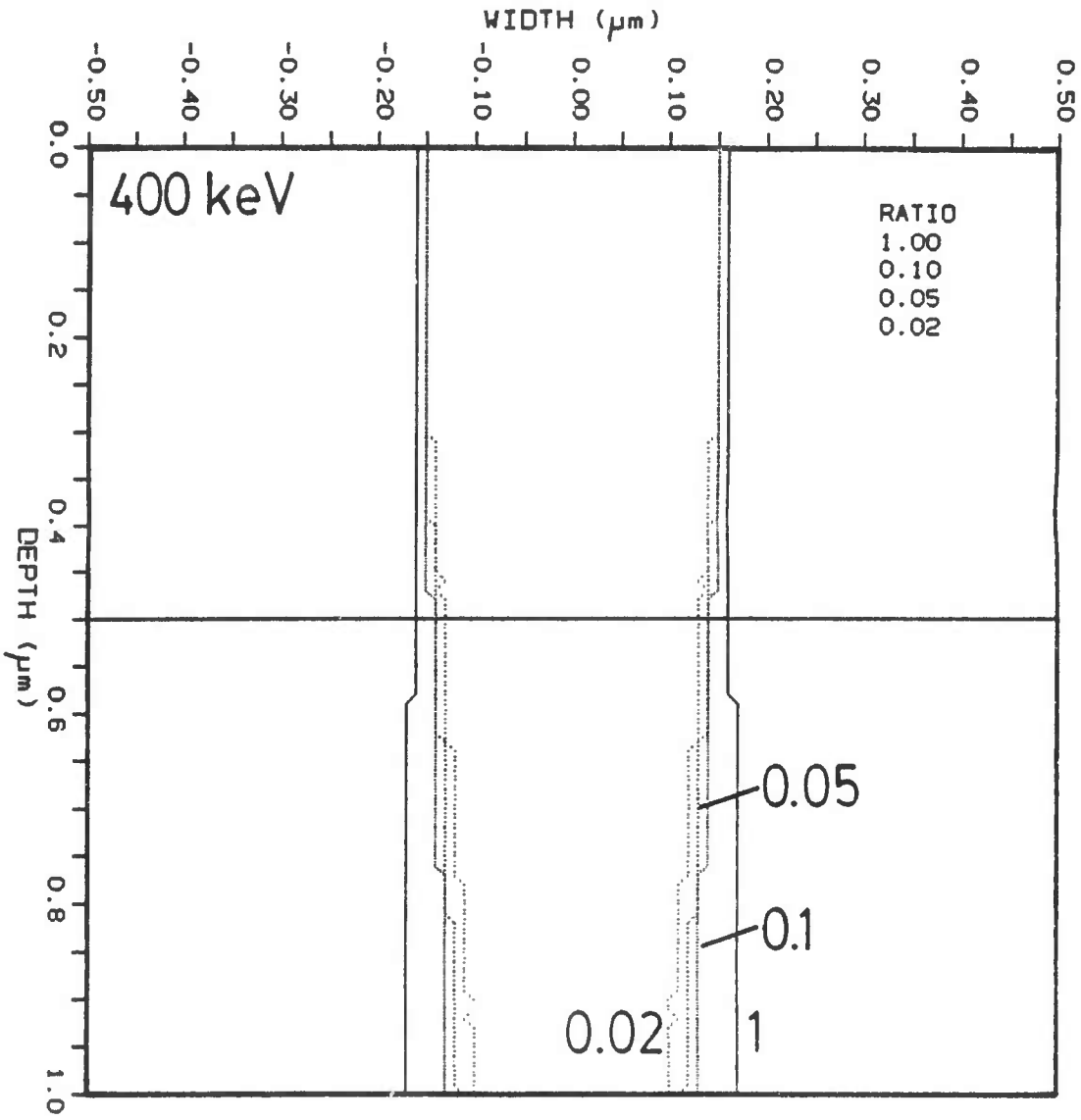


Figure 42 Deposited energy distribution for masked ion exposure for 400 keV incident ion energy and a mask width of 300 nm. For additional information see caption of Fig. P3.

least suitable one for the OGST fabrication.

2.2.1.4 Self-Aligned Dual Surface X-Ray Lithography

Self-aligned X-ray exposure of backside resists is in principle similar to conventional X-ray lithography, except that the substrate replaces the X-ray membrane and that no gap exists between the substrate and the mask. The X-ray absorption length in light targets, such as resists and semiconductors, is very small. For example for the Cu_L line with a wave length of 13.3 A the absorption coefficient for both Si and PMMA is about 0.5 μm^{-1} [18]. X-rays thus allow much thicker substrates than electrons and ions. The geometrical errors in the present dual surface X-ray exposure are extremely small because of the small separation between the lower surface of the absorber mask and the top surface of the resist. For an X-ray source size of 3 mm, a source-to-absorber separation of 50 cm, and a field size of 1 mm, the penumbral blur [19] equals 3 nm and the lateral magnification error [19] 1 nm for a membrane thickness of 500 nm. Self-aligned dual surface x-ray exposures are thus not limited by geometrical errors but rather by the photoelectrons, which are produced during the X-ray absorption process and which perform the actual exposure of the resist. The photoelectrons are likely to travel prependicular to the direction of flight of the incident X-rays in the plane of the resist [20]. The range of photoelectrons for soft X-rays is of the order of 20 nm [20, 21]. One thus expects a loss of linewidth of the order of 20 nm per edge in self-aligned dual surface X-ray lithography. X-rays are thus best suited for the highest resolution requirements and thick membranes.

2.2.2. Device Simulations (A. Perera and J.P. Krusius)

2.2.2.1. Influence of Device Structure on Operation

A cross-section of the idealized OGST is given in Fig. 43. A typical 60 GHz design of the OGST will serve here as the reference case for most of the discussion. This design is based on a n-type uniformly doped GaAs active layer, and has a gate length of 0.3 μm, and an active layer thickness of 0.15 μm. Other device parameters are given in Table IV.

The numerical methods employed in the present finite difference device simulation have been described in greater detail in Ref. [22], and will be only briefly summarized here. The continuity, momentum balance, Poisson, and displacement current equations describe the state of the semiconductor. This set of coupled differential equations is solved using the finite difference method. The Scharfetter-Gummel algorithm [23] discretizes the current continuity equation, while Poisson's equation is solved using banded Choleski LU decomposition [24]. Time steps of about half the dielectric relaxation time and the half implicit scheme [25] are used for the time discretization. For typical solutions it is required that both current and charge are converged to within 1 percent. The local drift-velocity electric-field, $v_d(E)$, and diffusivity electric-field, D(E), formalism is used to describe the high field transport within the active layer. Due to the small dimensions of this active region, transient carrier effects would be non-negligible; thus, two different transport models are employed here. The first one is the conventional quasi-static model, which assumes that carrier behavior is locally described by steady state velocity-diffusivity field relations. The second model is based on the assumption that carriers are

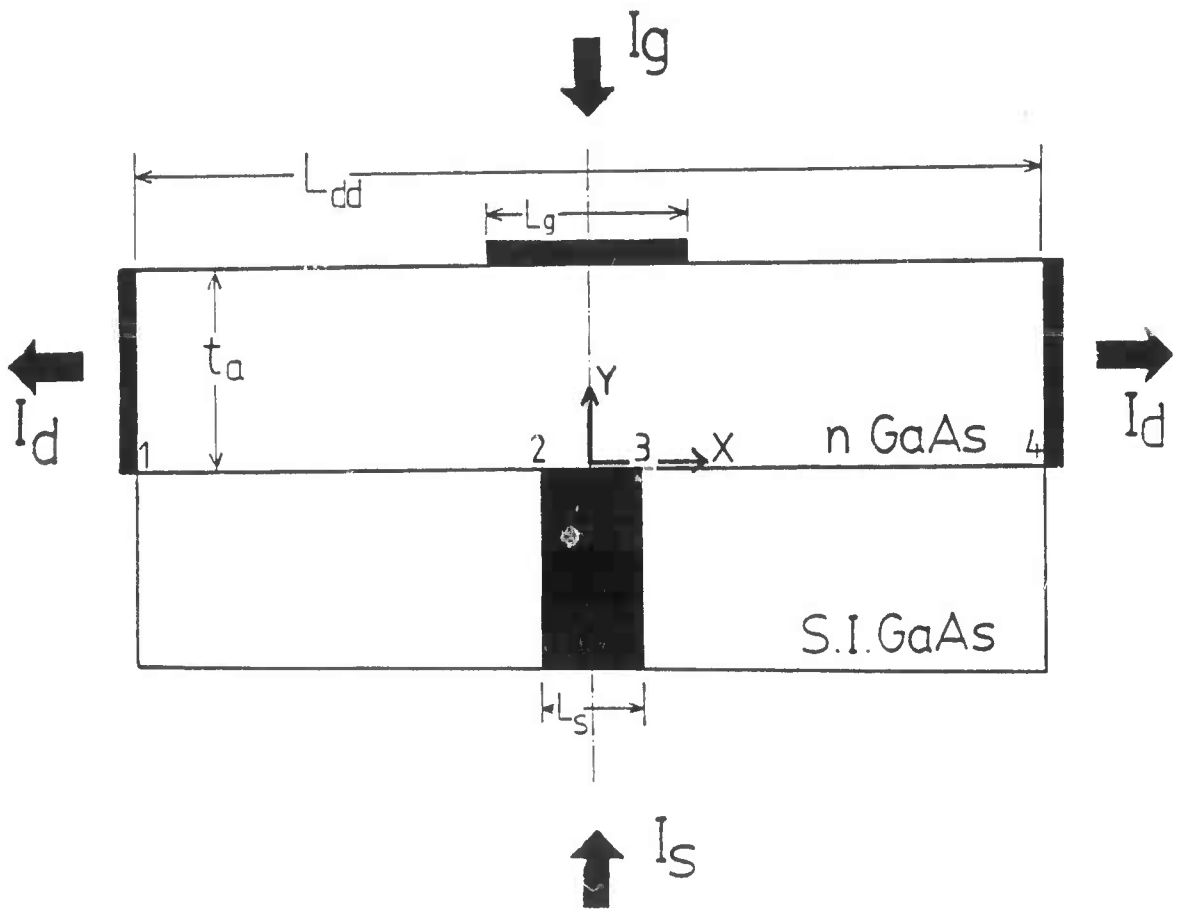


Figure. 43 Cross-section of the OGST. The coordinate system used in the simulation and the positive sense of the termial currents I_d, I_s, and I_g are defined here.

Table IV. OGST Device Parameters

Physical device parameters for OGST numerical simulation. (60 GHz design)		
L_g	=	300 nm
L_s	=	150 nm
L_{dd}	=	1.2 μm
t_a	=	150 nm
n_d	=	3.0×10^{17} cm^{-3}
Φ_b	=	0.8 V
ϵ_r	=	13.1

mostly undergoing transport in the central conduction band valley without sufficient time for scattering into the higher satellite valleys. The $v_d(E)$ and D(E) distributions for the former model are well documented, and a specific model similar to that in Ref. [26] is used here. The second transport model is contructed as follows. One-dimensional constant field Monte Carlo calculations have been employed to calculate the average drift velocity versus distance curves $v_d(x)$ for different E fields. The peak velocities of these curves are used to specify the $v_d(E)$ distribution. The associated diffusivity is obtained from the Einstein relationship. It is clear that this transport model mimics the near ballistic domain, and that it has to be considered as an "upper limit" for carrier transport.

Some aspects of the operation of the OGST have been analyzed earlier [26]. These are : the DC characteristics of the device for low bias voltages, the pinchoff mechanism and preliminary figures of merit for discrete devive operation. Here we extend the analysis to cover full device characteristics for symmetric and assymetric steady state operation, and transient operation. We further explore the distributed mode in detail. Two non-idealities arising from device fabrication are also investigated. The first one of these arises from gate-source misalignment, which breaks the symmetry of the device, and the second one from band bending effects at the active layer-to-substrate interface.

(a) Symmetry

Since the structure of the OGST is symmetric about the center mirror plane through the source and gate contacts (Fig. 53), the electronic

characteristics have to reflect this symmetry as well:

$$n(-x,y) = n(x,y) \tag{1}$$

$$\phi(-x,y) = \phi(x,y) \tag{2}$$

$$J_x(-x,y) = -J_x(x,y) \tag{3}$$

$$J_y(-x,y) = J_y(x,y) \tag{4}$$

$$J_x(0,y) = 0 \tag{5}$$

$$E_x(-x,y) = -E_x(x,y) \tag{6}$$

$$E_y(-x,y) = E_y(x,y) \tag{7}$$

$$E_x(0,y) = 0. \tag{8}$$

Here J_x,J_y,E_y,E_y,n, and ϕ denote the current density in the x and y directions,the electric field in the x and y directions, the electron density, and the electrostatic potential respectively. The cartesian (x,y) coordinate system is defined in Fig. 43. It follows from Eqs. (6) and (8) that a line with zero electric field must exist in the mirror plane between the gate and the source electrodes [26]. Because of the continuity of the dynamic variables, a cylindrical low field region surrounds this line.

(b) Pinchoff

The lowering of the symmetry related low filed region toward the source contact, and the associated movement of the depletion region away from the gate, for decreasing gate bias values, constitute the pinch off mechanism. It can be seen from Fig. 44 that already for the gate-to-source voltage (V_{gs}) of -1.5V the low field region has almost coallased with the source contact. For V_{gs} smaller than -2.0V the low field region merges completely with the source. The pinchoff voltages for the near ballistic and quasi-static models are -6.0 V and -5.0 V

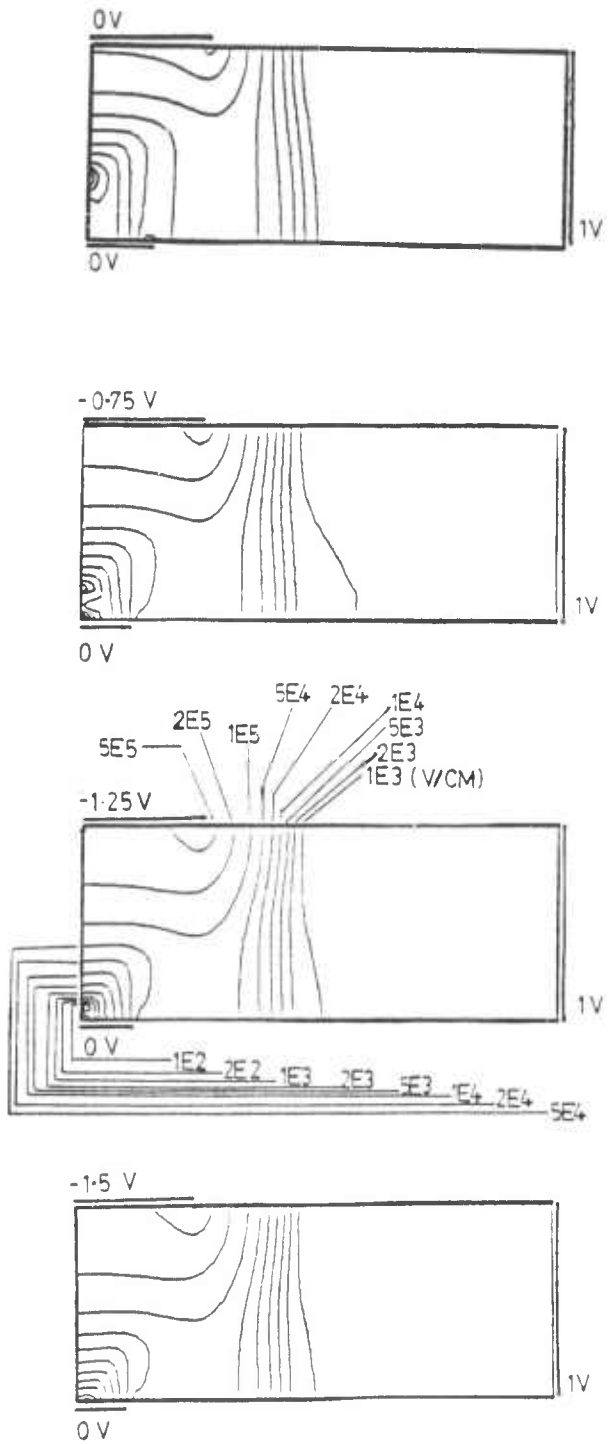


Figure. 44 Contour plots of the magnitude of the electric field for V_{gs} = 0,-0.75,-1.25,-1.5 V.

respectively, for the drain-to-source voltage (V_{ds}) of 3 V (Figs. 45a, 45b). The drain current for this device design depends linearly on the gate bias, a feature that is also evident from these graphs. This behaviour arises mainly from two-dimensional field effects and velocity saturation. From Fig. 45c we see that the entire channel region under the gate has an electric field larger than 20 (kV/cm). Since the critical field value for velocity saturation for GaAs is of the order of 5 (kV/cm), the velocity of charge carriers in this region would be saturated. Thus using a velocity saturated model to describe the current conduction in the channel and the one-dimensional depletion approximation to determine the thickness of the channel, one would expect a the drain to source current (I_{ds}) to depend on the square root of V_{gs}. In the present short channel OGST's, however, I_{ds} is modulated by the reduction of the source contact area for current collection due to the low field region in addition to the usual encroachment of the depletion region. These two factors together explain the linear pinch off behavior.

(c) Effective Gate Length

As stated earlier the OGST can be considered to be constructed by merging two MESFETs at their sources. This is illustrated in Fig. 46. Since the gate is placed above the source in the OGST, the effective active channel is confined to the region, where the gate extends over the source contact. This extension corresponds to $1/2*(L_g/L_s)$ for each side. Therefore, the effective channel length (L_{eff}) is controlled by the ratio L_g/L_s rather than L_g as in the MESFET. The simulated behavior of the drain-to-source current as a function of the gate-to-source

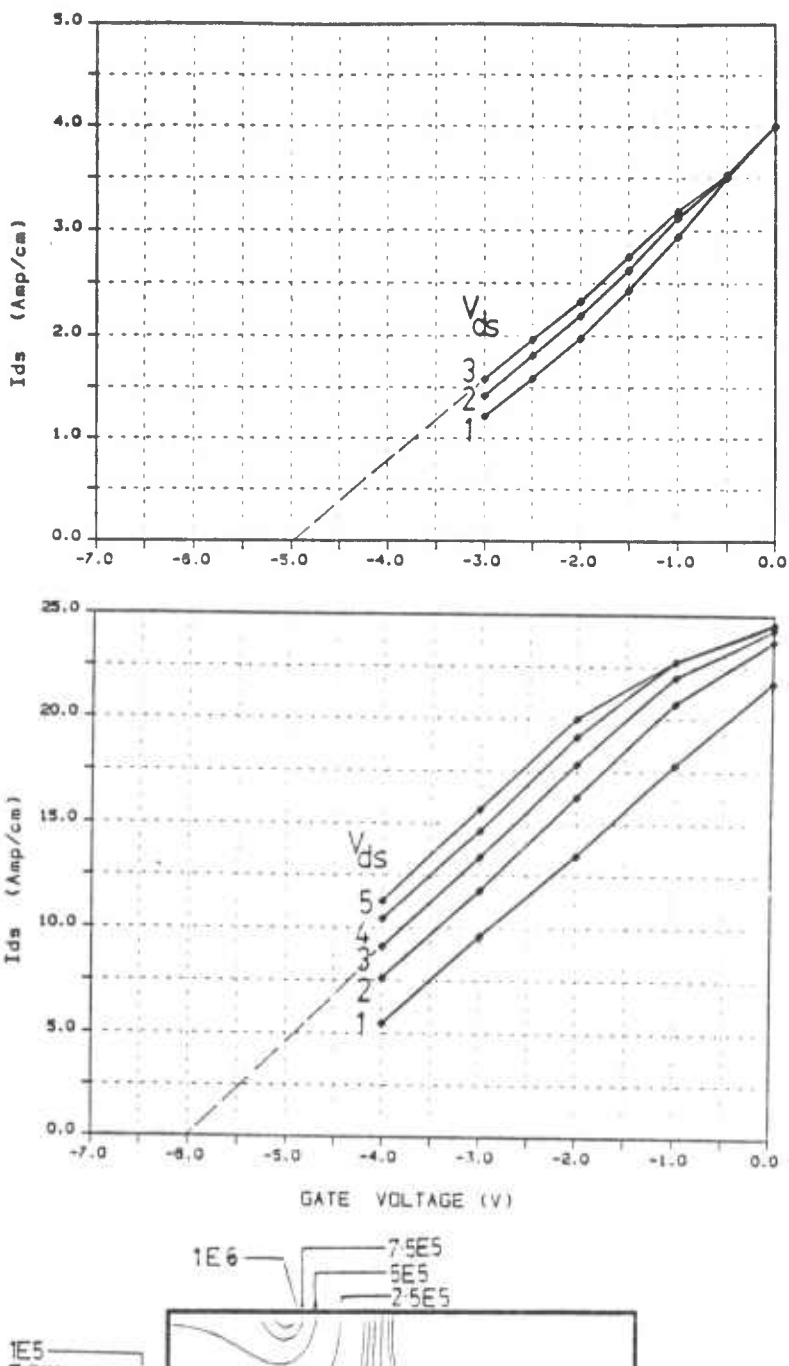


Figure. 45 The drain to source current (I_{ds}) as a function of the gate to source voltage (V_{gs}), for the quasi-static (a) and near ballistic (b) transport models. (c) Contour plot of the magnitude of the electric field for V_{gs} = -2.5V, and V_{ds} = 3V.

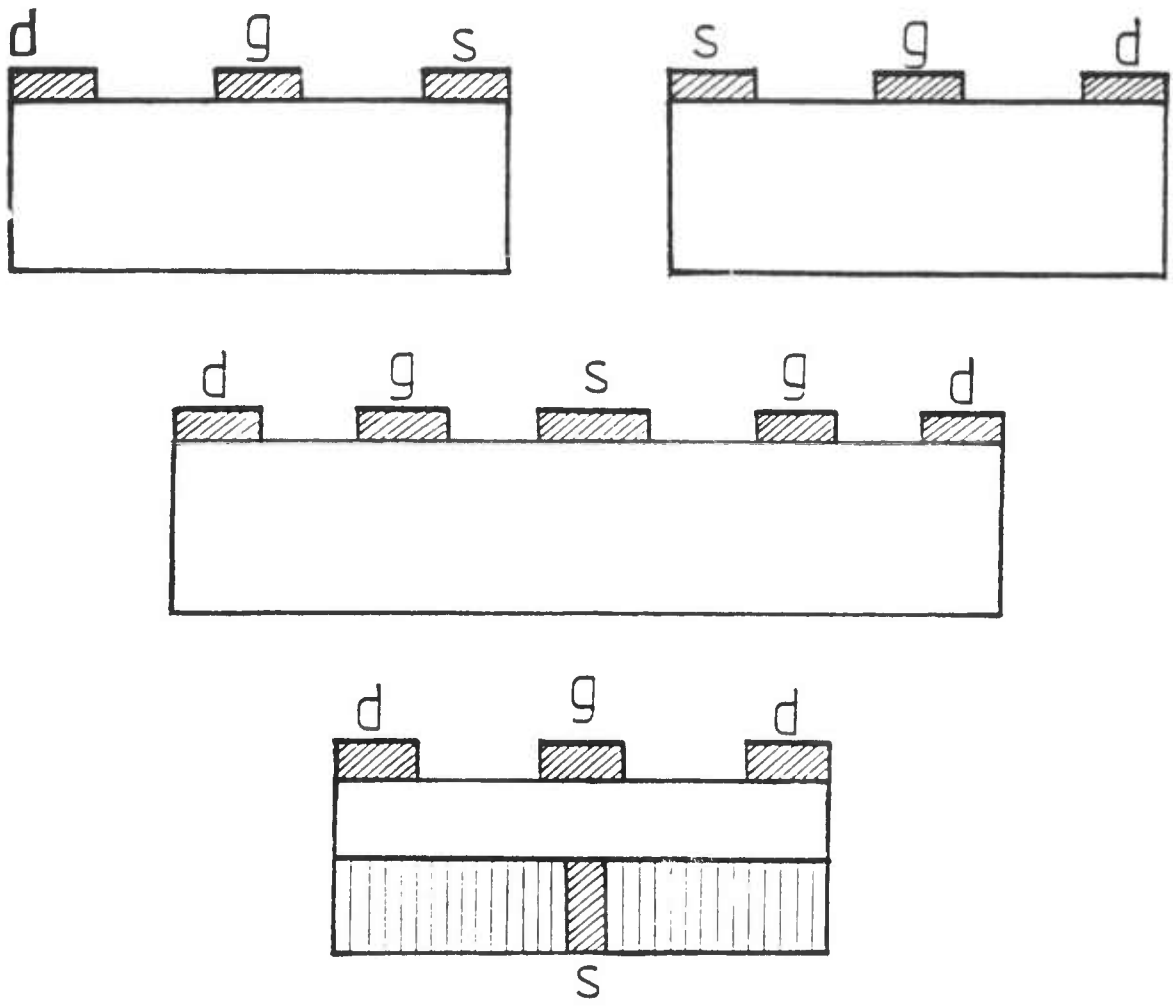


Figure. 46 The OGST seen as evolving from the joining of two MESFET's at the source ends.

voltage with L_{eff} as parameter illustrates this point (Fig. 47a). For example, the transconductance (g_m) of the device increases sharply with increasing L_{eff} instead of depending on L_g (Fig. 48a). Gate-to-source extension or L_{eff} values larger than zero are clearly needed for efficient channel current modulation (Fig. 47a). The gate-to-source capacitance (C_{gs}), on the other hand, depends on the gate length L_g. This is confirmed by the relative insensitivity of the derivative of the simulated stored charge (Q_T) with respect to L_{eff} over a wide range of V_{gs} values as shown in Fig. 47b. A more direct illustration for a single operating point is given in Fig. 48b. Since the cut off frequency (f_T) depends on the ratio of g_m and C_{gs}, it is limited by g_m for small values of L_{eff}, and by C_{gs} for large values of L_{eff}. Therefore an optimum value for the cut off frequency of the OGST is expected for moderate gate-to-source extensions. The simulated result for the present device parameters at the operating point V_{ds} = 3 V and V_{gs} = -2 V for this optimum is L_g/L_s equal to 1.8, which corresponds to an approximate L_{eff} of $1/2L_s$. This optimum value is insensitive to the actual operating point as long as the device remains in saturation.These conclusions are valid for both transport models, a confirmation of the fact that the overall qualitative behaviour of both transport models have been shown to be similar [17].

(d) Band Bending at Substrate Interface

Band bending at the active layer-to-substrate interface may have a significant effect on the characteristics of the OGST, since the current flow path near the source contact is close to this interface [26]. Band bending may be introduced by work function differences between the two

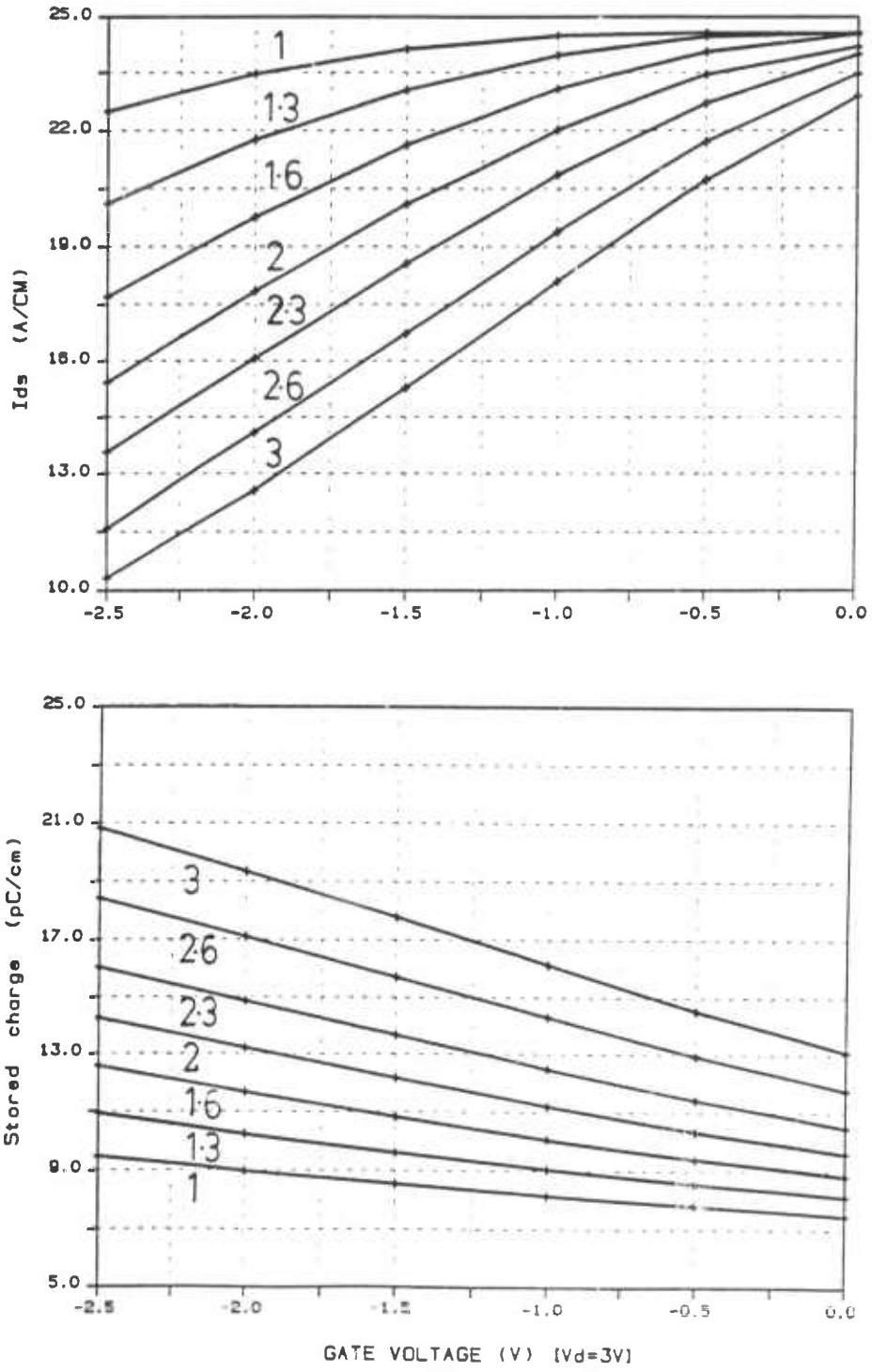


Figure. 47 I_{ds} (a), total stored charge in the device (Q_T) (b) as a function of the ratio (L_g/L_s), for V_{ds} = 3V, V_{gs} = -2V and (L_g/L_s) equal to 1,1.33,1.67,2,2.33,2.67 and 3.

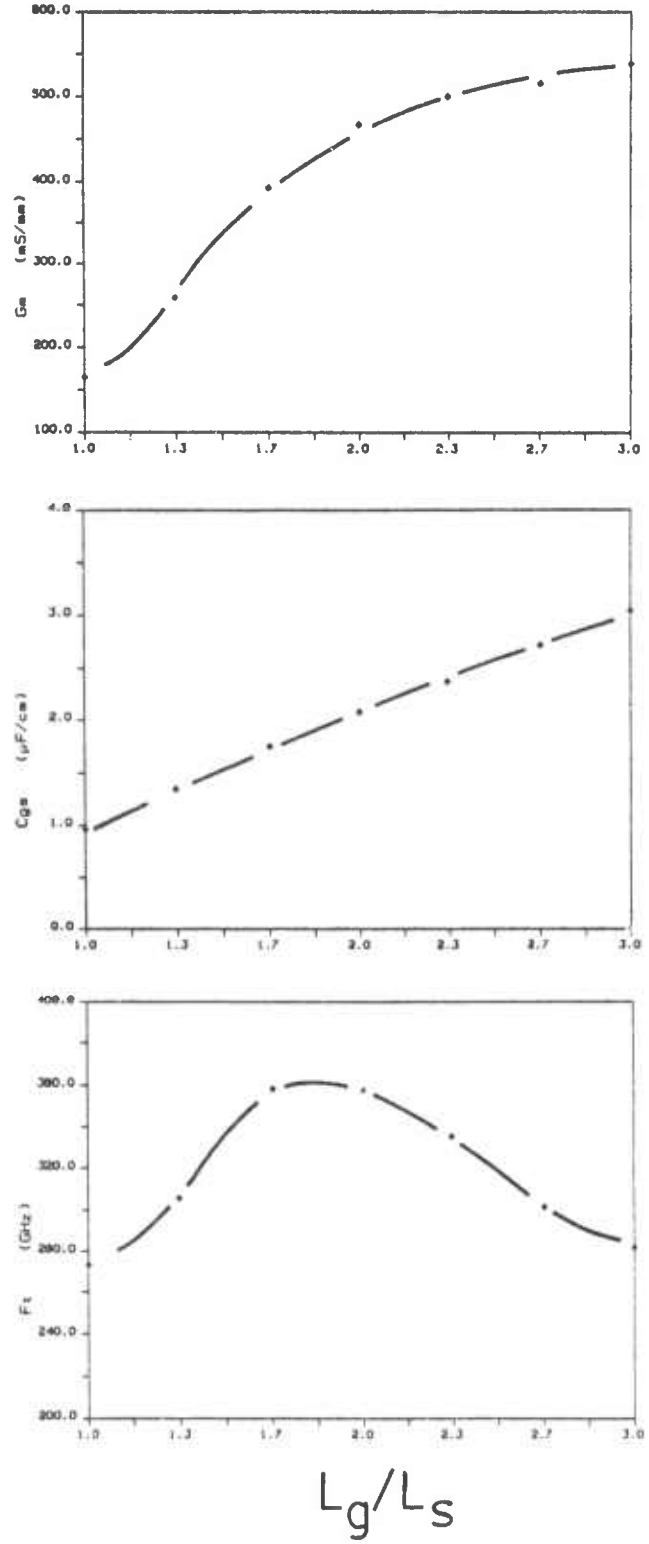


Figure 48 Transconductance (g_m) (a), gate to source capacitance (C sub gs) (b) and cutoff frequency (f_T) (c) as a function of the ratio (L_g/L_s), for V_{ds} = 3V, V_{gs} = -2V and (L_g/L_s) = 1,1.33, 1.67,2,2.33,2.67 and 3.

materials, fixed interface charge, variable interface traps, and back biasing. In the simulation band bending is modeled by an equivalent non-zero normal electric field (E_B) at the n-type GaAs and substrate interface. The full boundary conditions at this interface (1-2, and 3-4 in Fig. 43) are :

$$E_y = E_B \tag{9}$$

$$J_y = 0. \tag{10}$$

While a positive value of E_B enhances the carrier density, a negative E_B leads to a build up of charges. The simulation results for the drain current I_{ds} confirms the sensitivity of the DC device characteristics with respect to the back field (Fig. 49a). Small signal behavior is not as sensitive, since it, for fixed back fields, is determined by derivatives of the DC characteristics. This is illustrated in Fig. 49b for the total stored charge of the OGST. If one assumes that the back field were due mainly to fixed charge at this interface, then the values of E_B used in the simulations shown in Fig. 49 correspond to 0.02%, 0.2% and 2% of the number of surface atoms in one monolayer of GaAs. Fig. 50 shows g_m, C_{gs}, and f_T as a function of E_B. DC parameters, such as I_{ds}, are seen to change by as much as 40%, while only a 10% variation occurs in the value of small signal parameters, such as g_m and C_{gs}. The cut off frequency changes by a mere 5% for the large range of back fields between -50 and +50 kV/cm (Fig. 50c).

(e) Gate-to-Source Misalignment

The mirror symmetry of the ideal OGST assumes a perfect alignment of the gate and source electrodes. Both the operation and superior performance of the OGST depend on this feature. Even a small misalignment

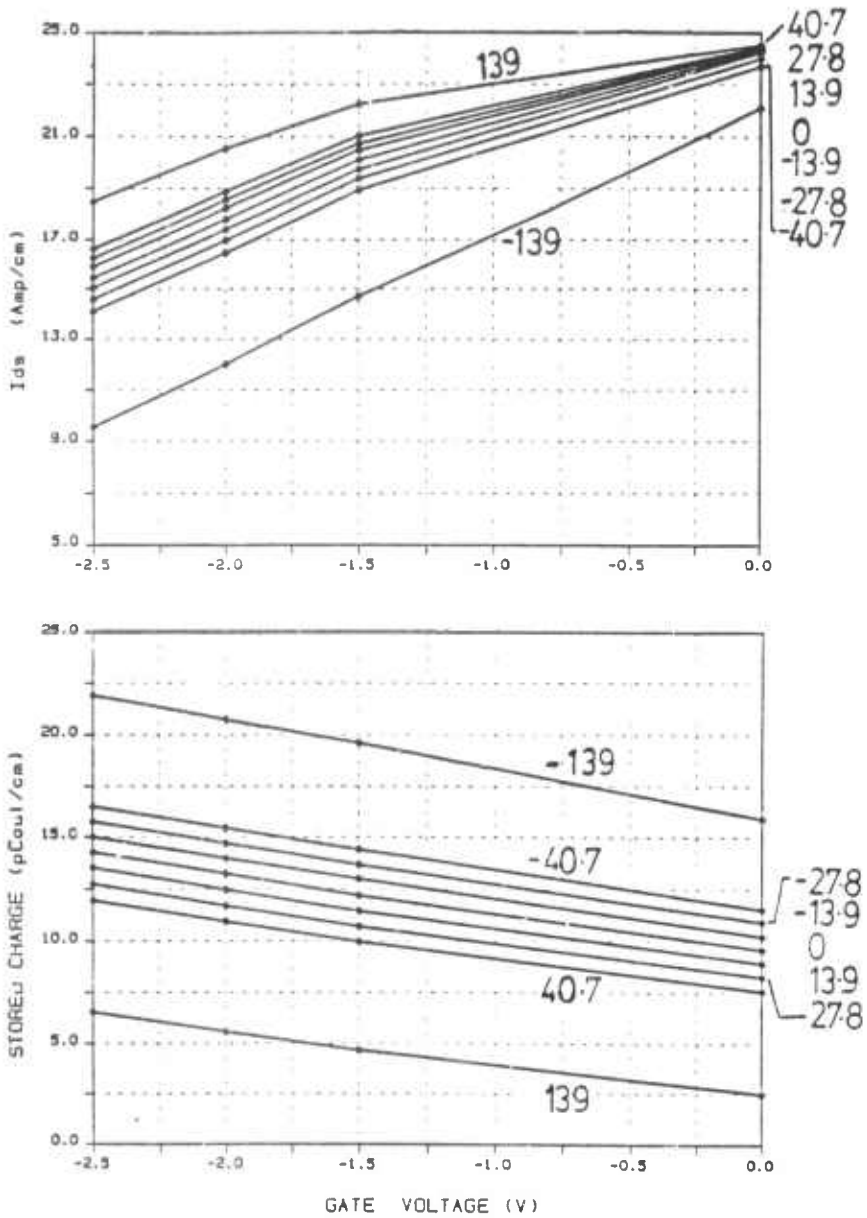


Figure. 49 I_{ds} (a) and Q_T (b) as a function of V_{gs}, for V_{ds} = 3V, and the interface back-electric field (E_B) equal to (+/-) 13.9,27.8,40.7,139.0 (kv/cm).

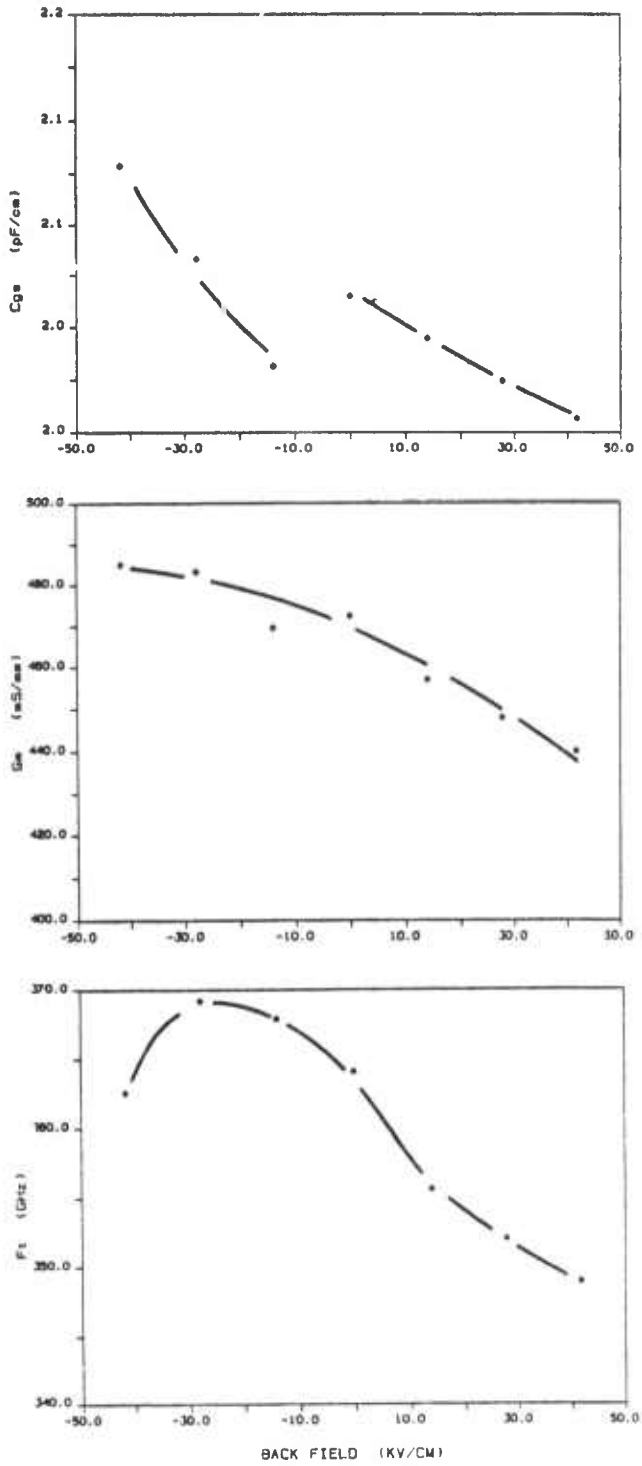


Figure 50 g_m (a), C_{gs} (b) and f_T (c)as a function of E_B See Fig. 49 for details.

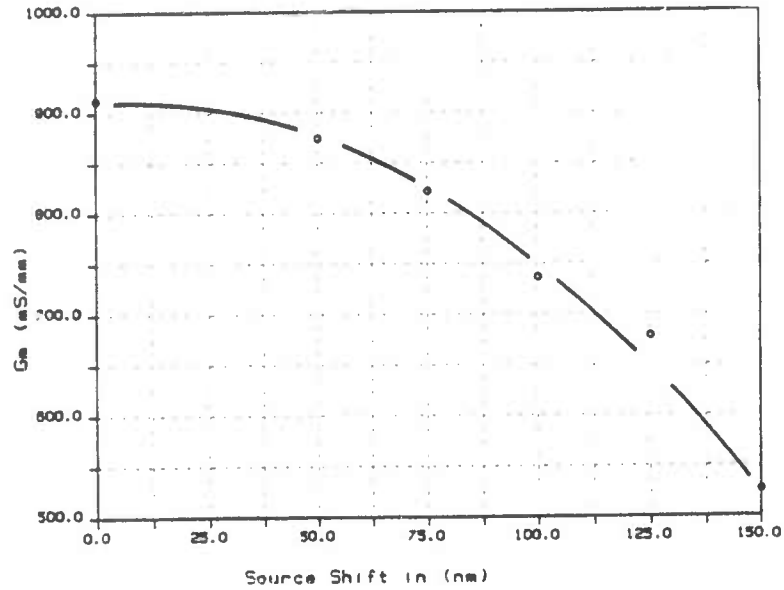
causes the gate voltage to modulate one of the drain current paths more than the other. For gross misalignment one of these current paths will approach resistive behavior and thus entirely lose the transistor effect. An illustration of the sensitivity of the OGST to gate-source misalignment is seen in Table V for L_g/L_s equal to 2. The source electrode has been misplaced by multiples of one third of the gate-to-source extension to the left. The magnitude of source current shows a net increase and the current density at the source electrode shows a rigid shift equal to the source misplacement, indicative of a soft symmetry violation. Despite of this g_m decreases rapidly as the source-gate overlap on one side decreases (Fig. 51a), an effect explained by two different effective channel lengths for the wo halves of the device. The modulation of the depletion region by V_{gs} will decrease as the source moves away from the symmetry axis. Thus, C_{gs} decreases slowly with increasing source misalignment as is illustrated in Fig. 51b. As the edge of the source contact moves outside the gate edge, the drain current modulation for the other half of the device drops virtually to zero and, the cutoff frequancy changes by over 40% (Fig. 51c). Hence, it is evident that the perfect gate-source alingnement facilitated by the self-aligned dual-surface lithography (Sec. 2.1) is indeed essential for the realization of optimum short gate OGST devices.

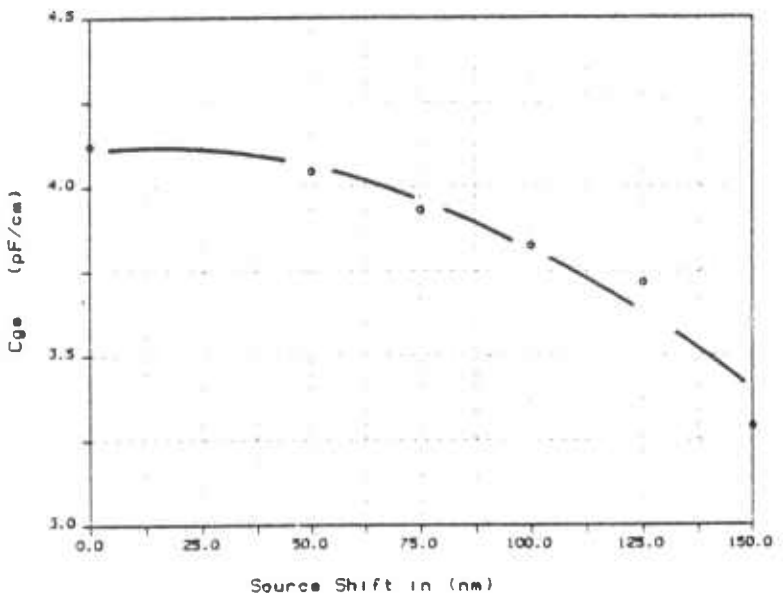
(f) Asymmetric Drive Conditions

In the normal mode of operation both drains of the OGST are driven symmetrically by equal voltages (Fig. 43). However, the OGST can also be operated by applying two different voltages on the drains. Such voltage assymmetries may also result from non-idealities related to device and

Table V. Effect of Source Misalignment

L_g = 300 nm, L_s = 150 nm, V_{ds} = 3 V.									
Shift of L_s towards the right drain terminal	Percent change in drain and source currents								
	I_{dr}%	I_{dl}%	I_s%	I_{dr}%	I_{dl}%	I_s%	I_{dr}%	I_{dl}%	I_s%
0 nm	-4.0	-4.0	-4.0	-17.0	-17.0	-17.0	-36.0	-36.0	-36.0
25 nm	-2.8	-4.2	-3.4	-14.9	-19.2	-16.9	-32.1	-39.4	-35.5
50 nm	-1.4	-4.7	-2.9	-10.9	-20.7	-15.0	-25.7	-42.5	-32.0
75 nm	-0.3	-4.4	-0.3	-7.4	-20.2	-11.1	-20.9	-42.3	-28.4
100 nm	0	-4.5	-1.3	-4.5	-20.7	-10.1	-15.5	-42.2	-25.1
125 nm	0	-5.0	-0.9	-2.5	-21.5	-8.2	-10.8	-44.4	-21.6
150 nm	0	-5.0	-2.0	0	-20.3	-4.2	-4.0	-43.4	-14.89
V_{gs} (V)	-0.5			-1.5			-2.5		





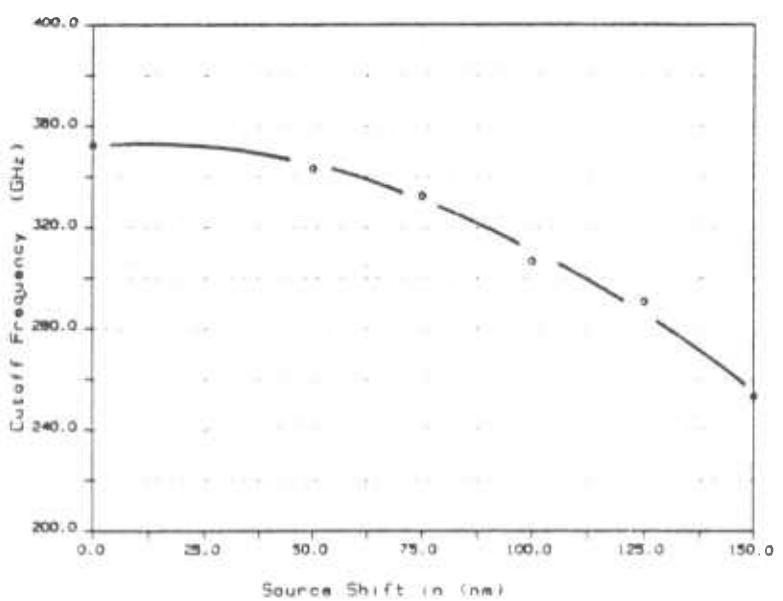


Figure 51 g_m (a) , C_{gs} (b) and f_T (c) as a function of net shift of the source contact away from the central axis, towards the right drain (ΔL_s), for V_{ds} = 3V, V_{gs} = -2V.

peripherial circuit fabrication, or from unequal phase velocities during distributed operation. Assymmetric drive conditions have therefore also been simulated. As one of the drain voltages is increased relative to the other, the current at the side with the larger voltage increases nonlinearly (Fig. 52a). This is because the effective source area for current collection is already pinched off for V_{gs} less than -2 volts, as was seen earlier, and thus any increase in either drain voltage causes a less than linear change in I_{ds}. The overall modulation of the total source current, therefore, remains nearly constant and g_m changes a mere 5% change for the large range of assymetric drive conditions, $V_{dr} - V_{dl}$ = 3 to 0 Volts (Fig. 52b). Thus the small signal behaviour of this transistor will be quite insensitive to the degree of symmetry of the drain voltages. This is confirmed in the plots of C_{gs} and f_T .vs. $(V_{dl}-V_{dr})$ (Fig. 52 b&c). Therefore, assymmetric drive conditions will mainly affect the dc behaviour of the OGST, and that being an increase in I_{ds} with the net voltage at the drain terminals.

2.2.2.2 Transient Response

The transient response of the OGST has been explored here by applying step pulses either on the gate or the drain electrodes and simulating the transient behavior of the device. A [illegible]mum time step of 2.5 fs has been used and steady state is in all c[illegible]hed in less than 1200 steps at about 5 ps. The gate step response of the terminal currents, I_d, I_s, and I_g, for a gate pulse from 0 to -2V with V_{ds} set at 3 V is given in Fig. 53. (Note that the directions of positive current flow for I_g, I_s and I_d are defined in Fig. 43) The terminal currents plotted

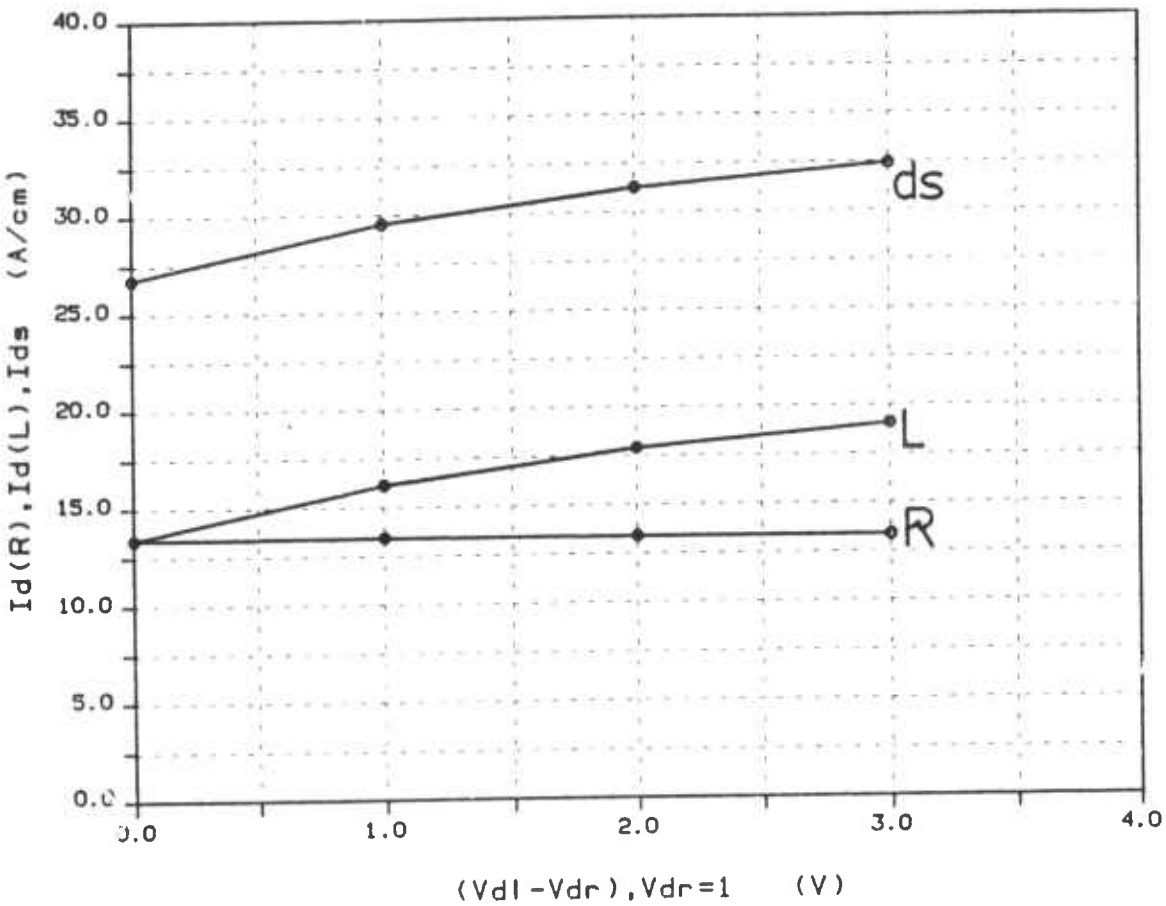
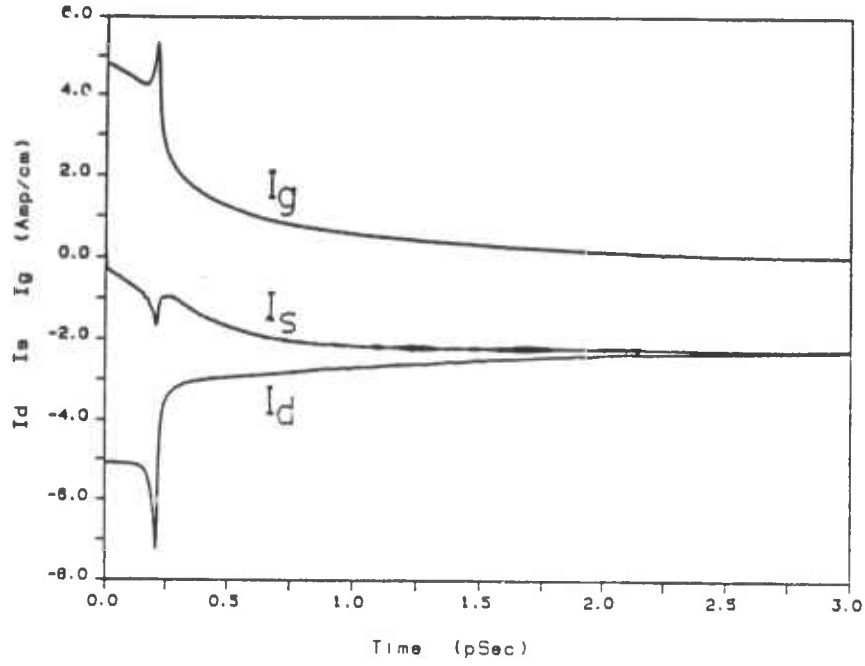


Figure 52 Current at the right drain terminal (I_{dr}) , current at the left drain terminal (I_{dl}) and the total source current (I_s) as a function of the difference between the voltage at the left and right drain ($V_{dl}-V_{dr}$), for V_{dr} = 1V .



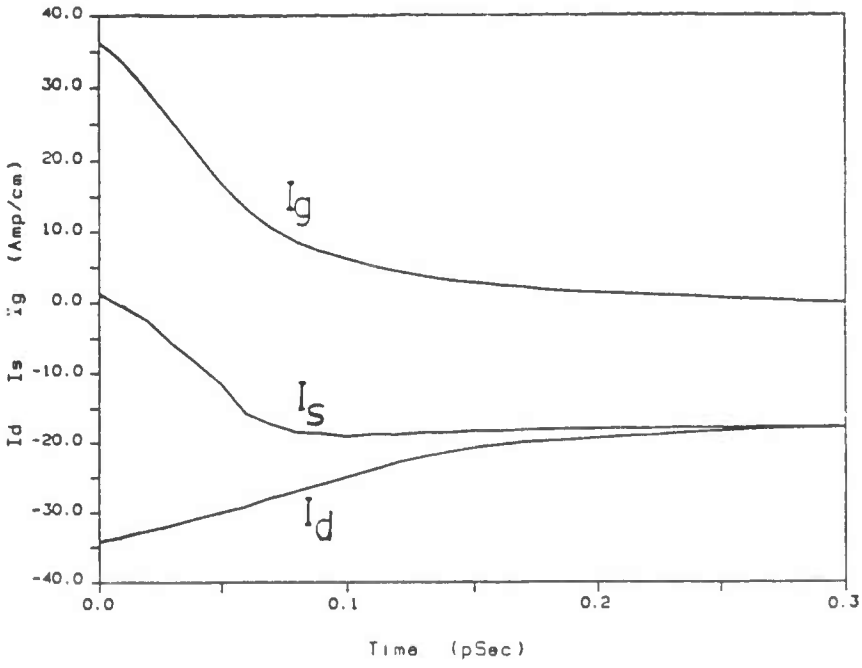


Figure 53. Terminal currents at the drain (I_d) (a), source (I_s) (b) and gate (I_g) (c) as a funtion of time, for a gate step, (V_{ds} = 3V, $V_{gs}(0)$ = 0V, $V_{gs}(0^+)$ = -2V), using 'ballistic' and quasi-static transport data, respectively. See Fig. 43 for positive directions of the currents.

contain contributions from the particle and displacement components for both transport models. In both cases the response has two distinct regions similar to what has been found to be the case for MESFET's as well [22]. The initial fast transient lasts 100 fs and 500 fs, and the slow exponential type second phase ends at 300 fs and 2 ps for the near-ballistic and quasi-static models respectively. In the initial transient charges inside the device redistribute without changing the net charge balance of the device too much. In the second phase the terminal currents and the total net charge adjust to their steady state values.

During the fast phase a large displacement current is seen leaving the gate whilst the both the source and drain currents enter the device. This behaviour can be explained by observing the time sequence of contour plots given in Fig. 54-57 . In both cases this period is characterized by the forming of an accumulation region at the drain side of the source contact. High-field velocity saturation effects can be associated with the forming of these regions for both transport models, and in the quasi-static case it will be due to differential negative mobilty caused at high electric fields as well. The depletion region does not, however, undergo much change during this phase. As more excess charge flows out of the source this accumulation region spreads across the entire source. The intital transient is caused by majority charge carriers rolling down the potenial hill under the gate, that forms when the voltage is stepped. Due to the definition of positive current flow that has been used, this flow of electrons into the source and drain causes $|I_d|$ and $|I_s|$ to increase and decrease, respectively (Fig. 53). The

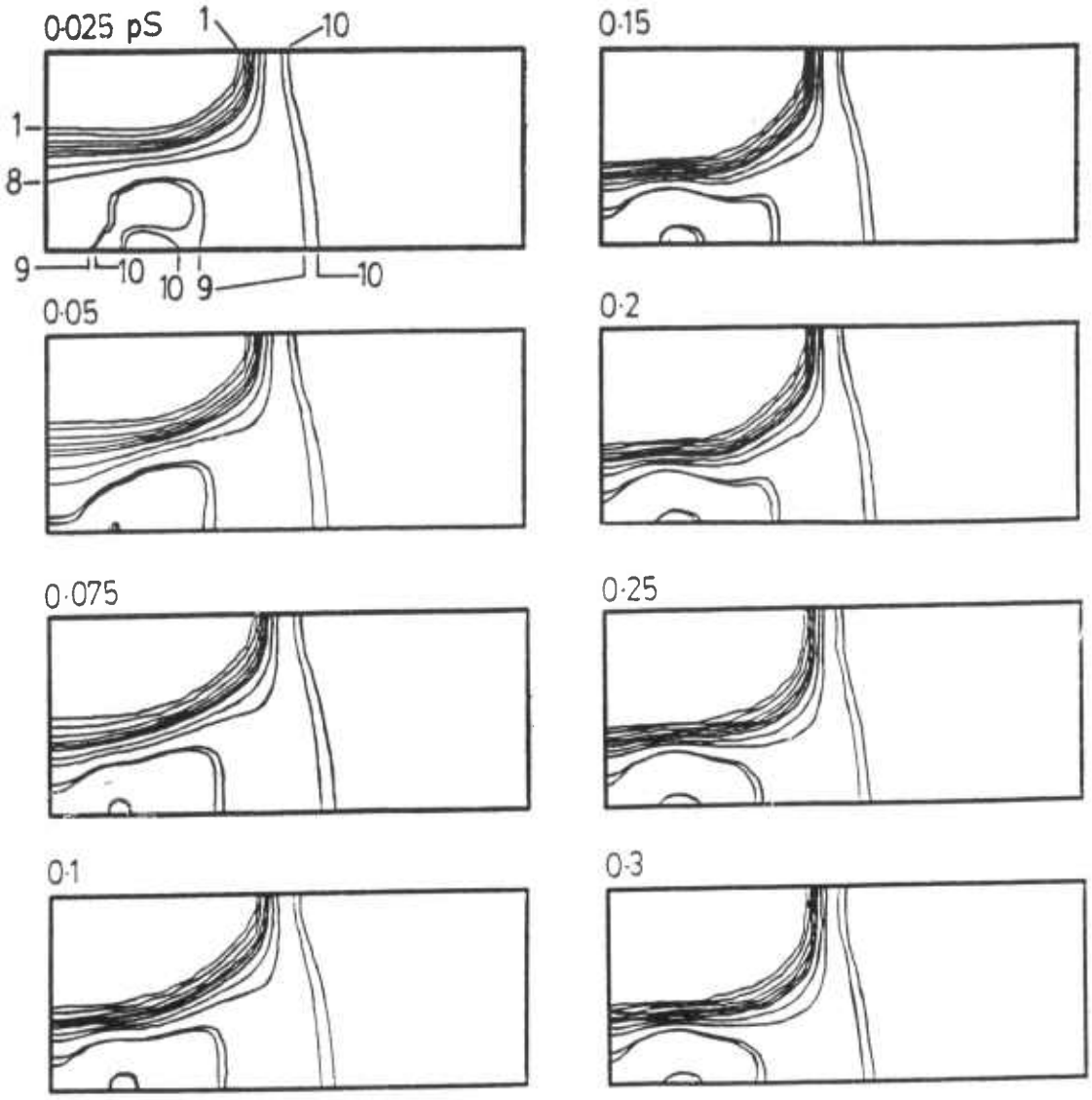


Figure. 54 Contour plots of the mobile carrier density (n) for t = 0.025, 0.05,0.075,0.1,0.15,0.20,0.25,0.3 (psec) for a gate step, (V_{ds} = 3V, $V_{gs}(0)$ = 0V, $V_{gs}(0^+)$ = -2V), using the 'ballistic' transport data. The values of the contours 10 down through 1 are 2.9,2.8,2.0,1.5,1.0,0.8,0.6,0.4,0.1,0.05 ($x10^{17}$ cm^{-3}).

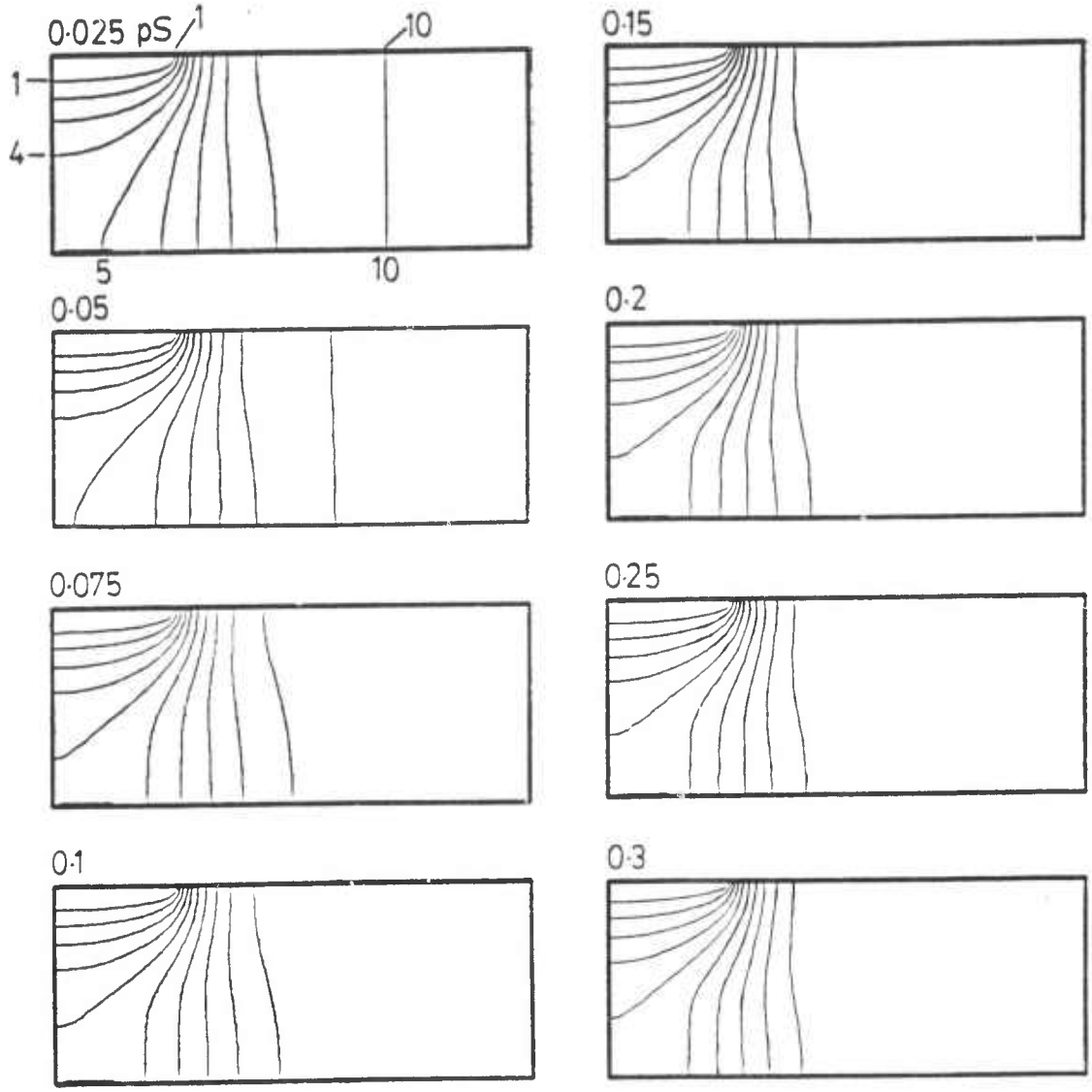


Figure. 55 Contour plots of the electro-static potential (Ψ) for t = 0.025,0.05,0.075,0.1,0.15,0.2,0.25,0.3 (psec) for a gate step, (V_{ds} = 3V, $V_{gs}(0)$ = 0V, $V_{gs}(0^+)$ = -2V) using 'ballistic' transport data. The value of the contours 10 down through 1 are 2.5,2,1.5,1,0.5,0,-0.5,-1,-1.5,-2 (volts).

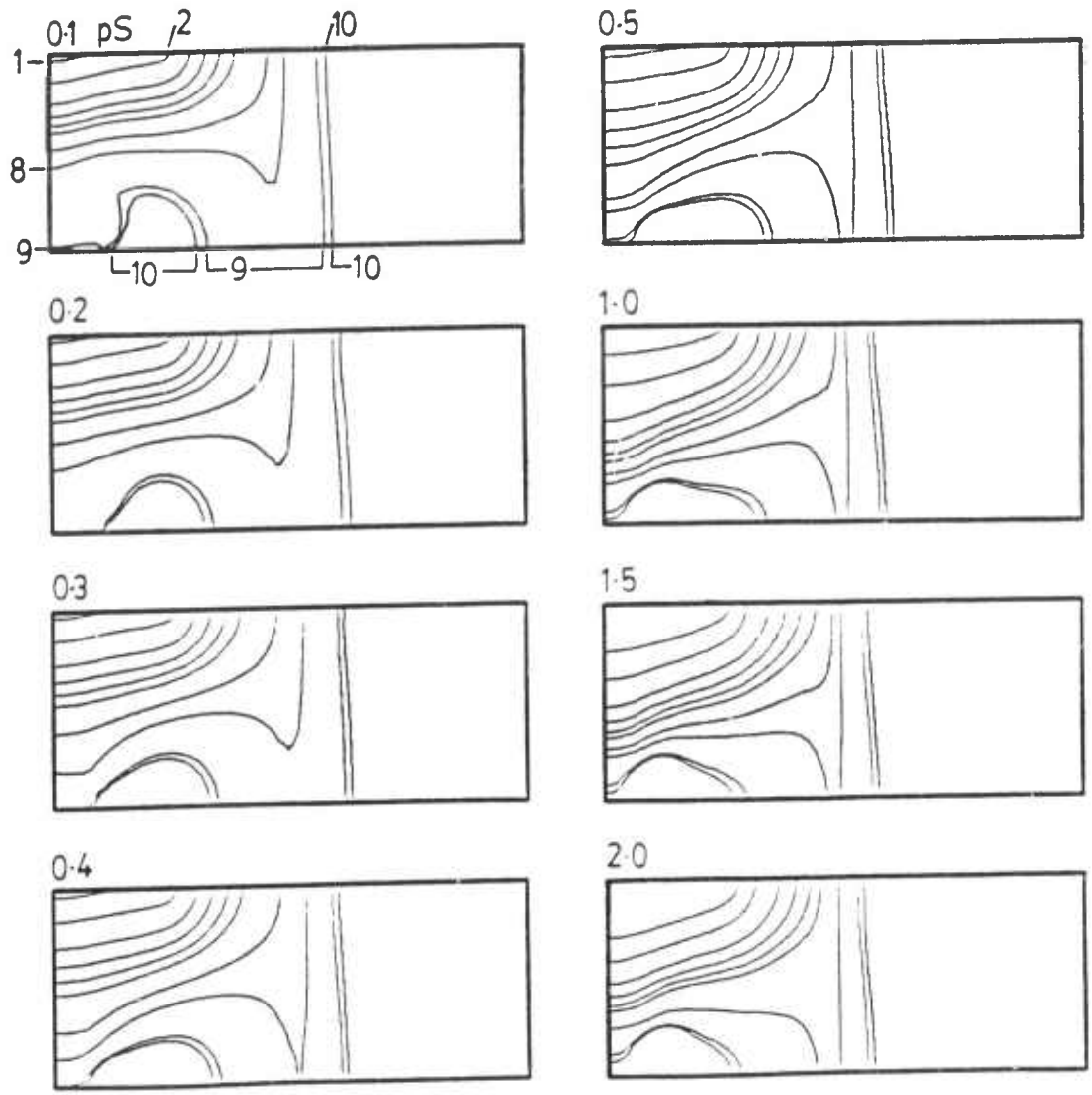


Figure. 56 Contour plots of the mobile carrier density (n) for t = 0.1, 0.2,0.3,0.4,0.5,1.0,1.5,2.0 (psec) for a gate step, using quasi-static transport data. See Fig. 54 for details of contours.

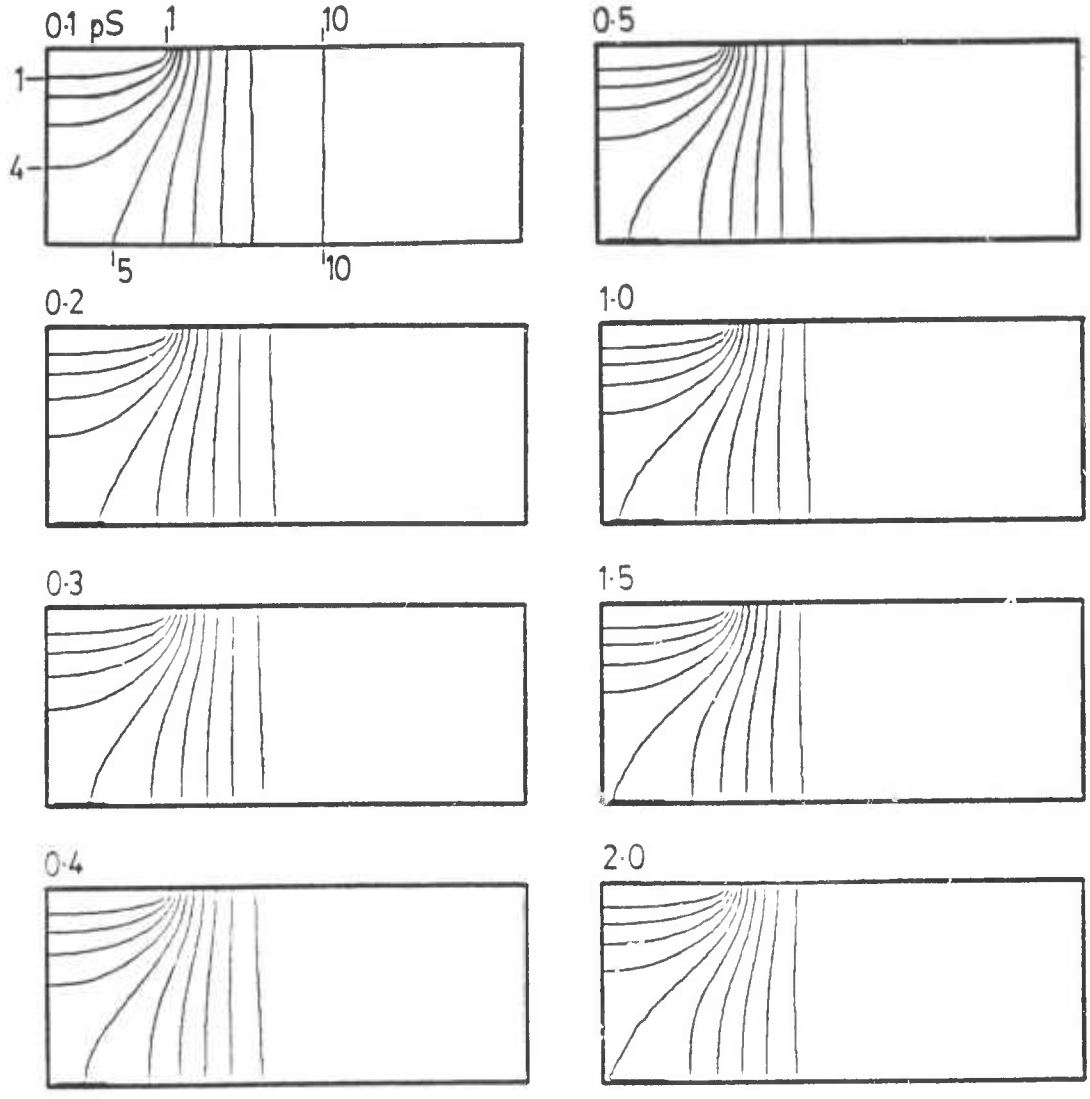


Figure. 57 Contour plots of the electro-static potential (Φ) for t = 0.1, 0.2,0.3,0.4,0.5,1.0,1.5,2.0 (psec) for a gate step. using quasi-static transport data. See Fig. 55 for details of contours.

cause for the difference in speed for the two cases is clearly model depenadant, but can also be seen in looking at the changing of internal potential contours of the device with time. In the "ballistic" transport model the zero potential contour sweeps under the gate and creates a steeper potential energy hill. The potential gradient under the gate does not change in the initial phase for the other model, and this added driving force is, therefore, not present. In the slower phase, whilst the accumulation regions remain unchanged, the depletion regions steadily extend out to the equilibrium values as more majority carriers leave the device. The gate current slowly decays to zero and the magnitude of the source and drain currents move closer towards equality. This could be interpritted as the charging of the gate-source capacitance.

The drain step response is examined by stepping the drain voltage from 1 to 5 volts, while keeeping the gate at ground. Since the device is already in saturation for V_{ds} = 1 V, I_{ds} does not change by very much. The transient terminal currents I_d, I_s and I_g for such a drain voltage step are plotted in Fig. 58 . Here, while the source current remains relatively constant the gate and drain terminals have electrons flowing out and into them, respectively. In this case too an initial fast phase is followed by the gradual adjustment of the currents to their steady-state values. The basic driving forces during this transient is seen in the contour plots of mobile charge density, and electrostatic potential (Fig. 59 and 60).

2.2.2.3 Distributed Amplification

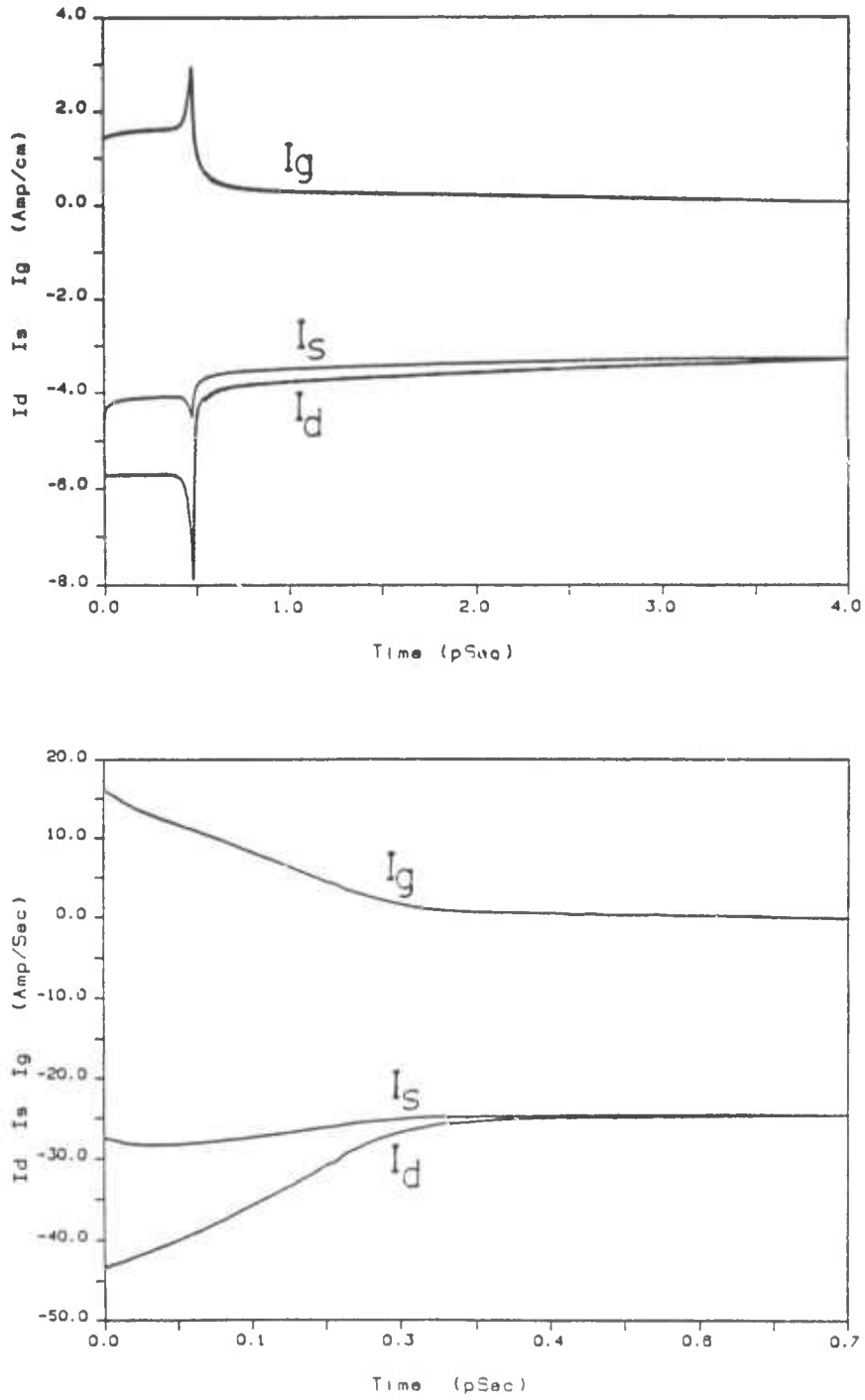


Figure. 58 The terminal currents I_d, I_s, and I_g for a drain step, as a function of time. (V_{gs} = 0V, $V_{ds}(0)$ = 0V, $V_{ds}(0^+)$ = -2V), using the 'ballistic' (a) and quasi-static (b) transport data.

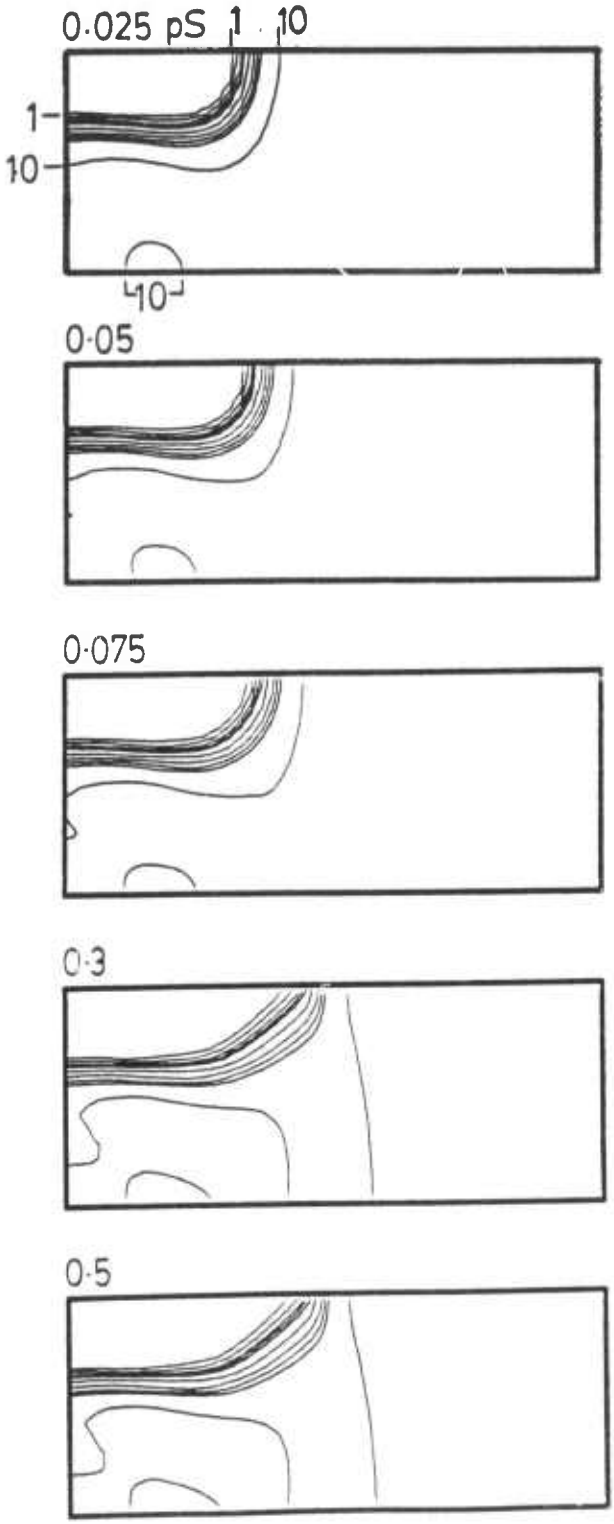


Figure. 59 Mobile charge density contour diagrams as a fuction of time for a drain step response, for t = 0.025,0.05,0.075, 0.25 and 0.3 psec. See caption of Fig. 54 for details of contours.

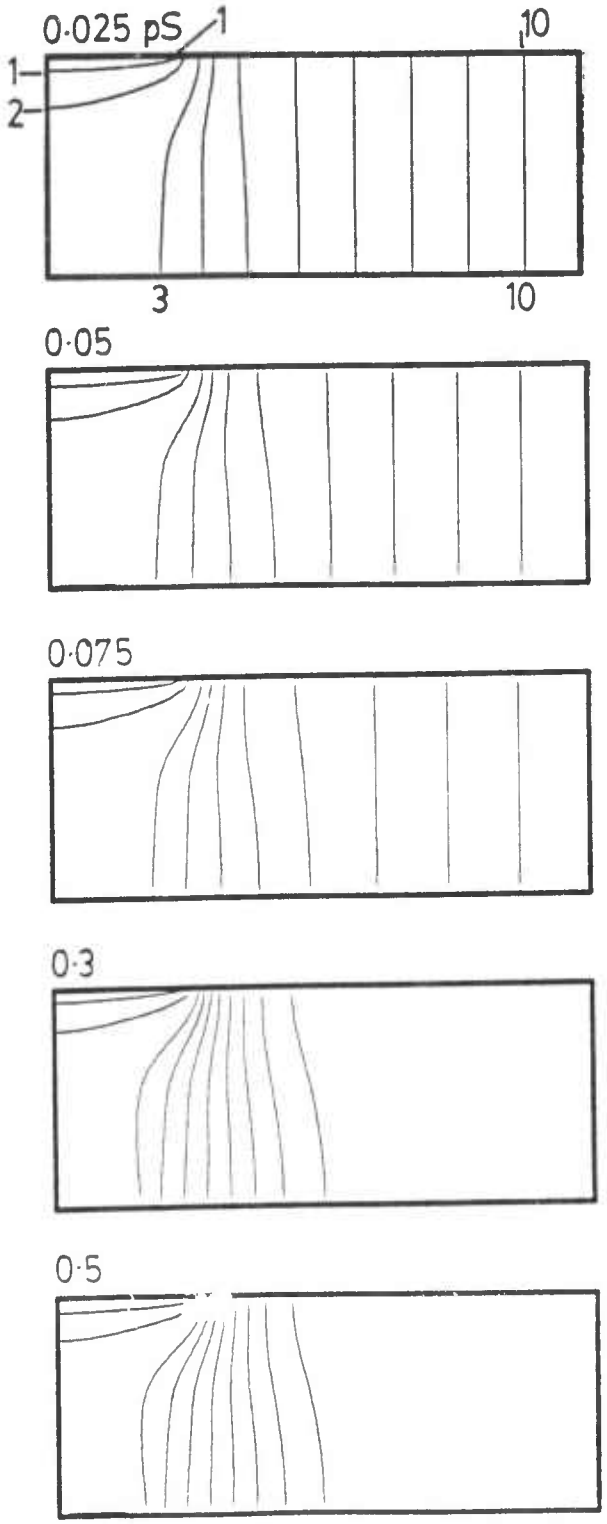


Figure. 60 Electrostatic potential contour diagrams as a function of time for drain step response, for t = 0.025, 0.05, 0.075, 0.25, and 0.3 psec. See Fig. 55 for details of contours.

In each cross section, taken along the current flow, the structure of the OGST can be considered to consist of three coupled microstrip lines. The gate line runs symmetrically between the two drain lines over the ground plane (source). If the input signal is fed into the gate line, the output signal on the drain lines builds up as the waves travel along the width direction of the device. The OGST can thus act as a distributed amplifier, a unique capability of this device. The structure of the ideal OGST has a rotation symmetry of 180 degrees around a line placed into the center of the gate line along the width direction of the device. Thus also the coupling of the traveling electromagnetic waves must show this same symmetry. In the following the distributed amplification characteristics are analyzed by modeling the OGST as three coupled microstrip lines with the coupling determined by the FET and geometrical characteristics of the OGST. Both capacitive coupling, arising from the drain-to-gate feedback capacitance, as well as the transconductance coupling, the gain element of the OGST, are taken into account.

The top view of the structure of the OGST is shown in Fig. 61. In each infinitesimally short cross section the equivalent circuit for these transmission lines is given in Fig. 62a, which because of the rotation symmetry reduces to only two effective coupled lines (Fig. 62b).

The circuit elements g_m, C_{dg}, C_{ds}, C_{gs}, and g_{dd} arise from FET operation and can be calculated from the numerical two-dimensional device simulations described above. Conductances are derived directly from simulated current-voltage characteristics via divided differences. In

Figure 61 Top view of OGST device.

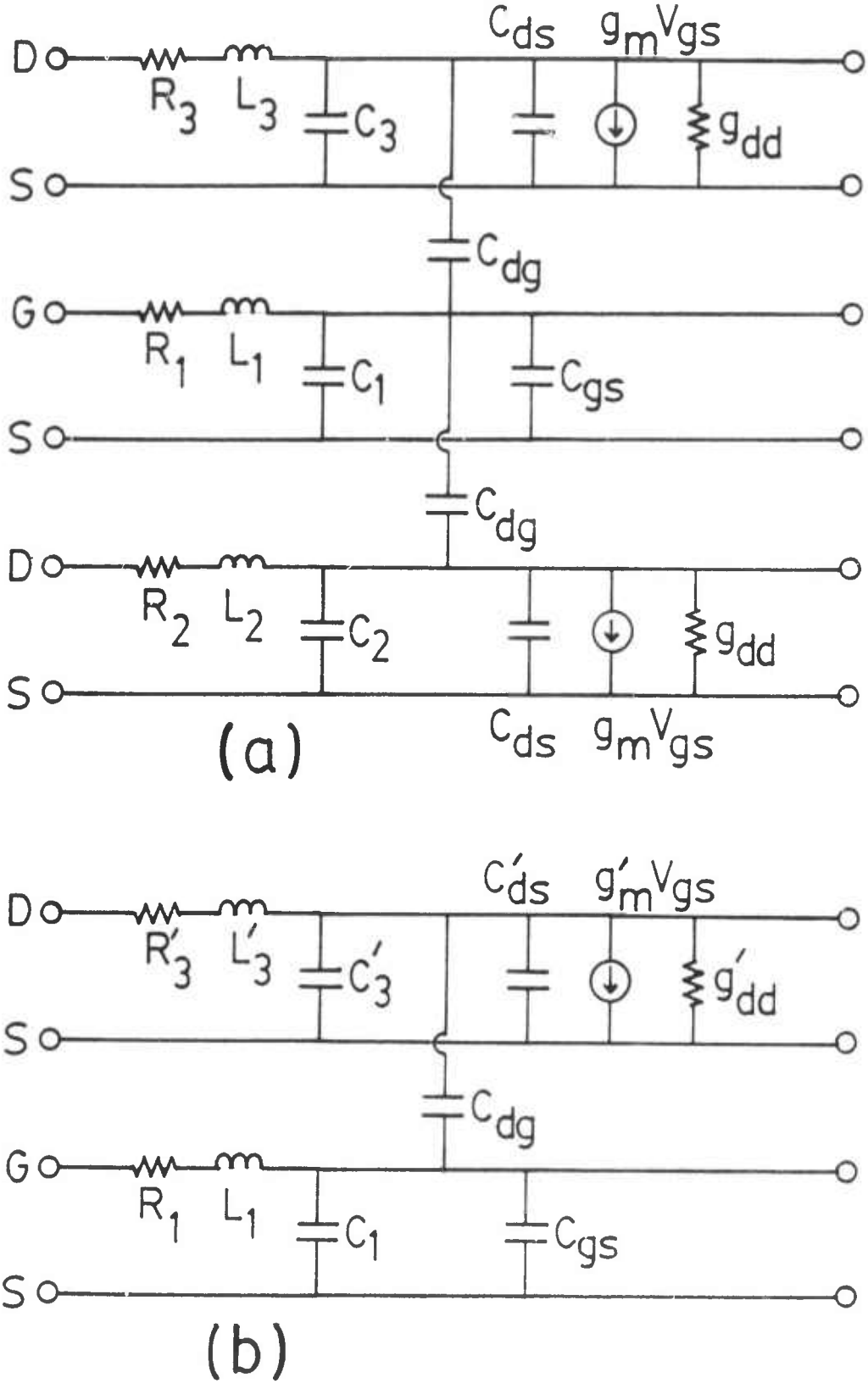


Figure 62 Equivalent coupled trnasmission lines model for OGST. (a) Both drain lines shown, and (b) with one effective drain line.

order the calculate the electronic contributions to the capacitances the total net charge within the device has been integrated for two adjacent operating points, and the capacitance then determined from the divided difference of the total charge with respect to the relevant terminal voltage changes.

The justification for treating the drain and gate lines of the OGST as classical low loss microstrip lines is based on the following heuristic arguments: (a) both lines are long compared to the width in the OGST cross section, (b) both lines are homogeneous in the length direction, (c) both lines are inhomgeneous in the width direction with an approximate mirror symmetry about the vertical bisector plane of each line, (d) both lines are low loss (line resistance small, and resistance to ground large). The coupling of these microstrip lines includes in principle both capacitive and inductive contributions. The latter coupling is, however, for practical purposes forbidden because of the reflection symmetry of the device structure. Inductive coupling of drain lines to the gate are strictly forbidden by symmetry, while the opposite is only approximately true because of the small gate currents. The geometrical coupling capacitance is small compared to the electronic gate-to-drain feedback capacitance and has hence been neglected altogether. The transmission line parameters R_1, R_2', L_1, L_2', C_1, and C_2' can then be calculated using formulas for microstrip lines [27,28].

The above model for the distributed interaction allows for even and odd modes of propagation. The basic transmission line equations are set up using an approach similar to the one followed by [29,30]. Ref. [31] had treated the same problem earlier but contained several algebraic and

conceptual errors, and hence drawn conclusions are unconfirmed. The transmission lines analysis leads in our case to a 4 x 4 complex linear system of equations of the form

$$A\,u = i,$$

where A is a 4 x 4 coefficient matrix with the units of admittance, u the 1 x 4 column voltage vector for the mode amplitudes, and i the 1 x 4 current vector. i has only one non-zero component because only the gate line is driven. Drain and gate line termination impedances are included in the admittance matrix. The propagation coefficients γ_1 (even mode) and γ_2 (odd mode) are determined by the impedance and admittance matrices. The complex linear system is solved by standard Gauss-Jordan elimination provided in the sortware package LINPACK. Further details will be given elsewhere [32].

Programming of the above approach has almost been completed, and software testing started. The results will be published elsewere when available [32]. The results from the coupled microstrip line analysis will be compared with two different approximations to the same problem. The first one is based on ideal lossless transmission lines with a constant transconductance coupling only. Analytical models of a lossy line with transconductance coupling and also with Miller capacitive coupling have been treated earlier by C. A. Lee and G. C. Dalman of Cornell University. The second one relies on circuit simulation with the assumption that each thin cross sectional slice of the OGST device is much faster than the speed of propogation along the lossy gate and drain lines of equal length. The circuit simulation results should, for short

cross sectional slices and low loss, converge to the coupled transmission line case. Finally, results can also be compared with a previous analysis performed by TRW [31]. These comparisons are currently in progress, and will facilitate, once completed, a thorough understanding of the distributed gain characteristics of the OGST. Future device and amplifier designs can be based on these results.

2.3 MICROWAVE DEVICE CHARACTERIZATION

As part of the program to characterize very small mm-wave devices, work was initiated on (1) the assembly and evaluation of scalar and vector semi-automatic swept frequency network analyzers for both Ka and W bands; (2) the development of waveguide to microstrip adaptors; and (3) the fabrication and characterization of very small transmission lines useful as interconnects between the device under test and the waveguide to microstrip adaptors. A discussion of the progress made is presented below.

2.3.1 Scalar and Vector Network Analyzers (G. C. Dalman, H. Kondoh)

Two scalar vector network analyzers have been assembled and tested, one for Ka band and one for W band. Both utilize broadband crystal detectors so that real time measurements of the magnitude of the scattering parameters of an unknown load can be made over a broad range of frequencies. Both oscillographic and x-y recorder displays are possible.

Work has also been completed on a computer-aided 4-port vector network analyzer for Ka band. A description of the first design of this analyzer is attached as Appendix III. This analyzer utilized two thermistors as power detectors. Since thermistors respond slowly, the testing time is relatively slow. In our recent second design broadband crystal detectors are being used as replacements for the two thermistors. While the operation of the analyzer is the same, this substitution has reduced the testing time significantly. It should be noted, however, that the speed of the newer design is limited by a mechanical phase shifter which is used in the system. In making a measurement it is necessary to make two frequency sweeps, one with the mechanical phase shifter set to 0° at the middle of the band and another with a 90° setting. The resetability of the fequency of the sweeper becomes an important factor limiting the measuring accuracy. However, the use of an electronic phase shifter which alters the phase between 0° and approximately 90° at each of the frequency steps will eliminate this problem. It will also shorten the test time since only one frequency sweep is required. The use of the electronic phase shifter, along with the two crystal detectors discussed above, would make quasi-real-time display of the results possible. Development work on the electronic phase shifter is under way.

Components for a 4-port W band network analyzer have been assembled and preliminary performance testing has started. Also an H.P.8510A automatic network analyzer has been received and is operational to 18 GHz. It is planned to use the HP equipment to determine the low frequency S-parameters of experimental transistors.

2.3.2 Waveguide to Microstrip Adapter Development (G. C. Dalman)

To facilitate the testing of very small transistor structures a precision waveguide to microstrip adaptor is needed. Our initial approach was to fabricate a waveguide-coaxial line-microstrip adaptor for Ka band. However,TRW (Redondo Beach, CA) has completed the development of a W-band finline waveguide to microstrip adaptor and they have supplied us with one of these fixtures. We have scaled their design to Ka-Band and the results are discussed below.

2.3.2.1 Ka Band Waveguide to Microstrip Text Fixture (J. Bellantoni, G. C. Dalman, C. A. Lee)

A waveguide to microstrip test fixture for testing devices at millimeter-wave frequencies (Ka-Band) has been realized using E-plane printed circuit technology. The transition is accomplished with an antipodal finline that rotates the TE_{10} waveguide field into a microstrip configuration [33]. Preliminary test results indicate excellent 1.3:1 VSWR at the 36 GHz center design frequency and suggest the possibility of better than 2:1 VSWR over the entire 26.5 to 40.0 GHz waveguide band. Figure 63 shows two views of this Ka-Band transition; the upper photograph shows the assembled fixture and the lower photograph shows it with the two top parts removed to each side of the bottom part. The patterned Duroid microstrip transition can be seen in the middle of the waveguide slot.

The test fixture consists of gradually tapered finline ridges on opposite sides of the dielectric substrate that concentrates and rotates the field. The dielectric selected for the test fixture prototype is 5

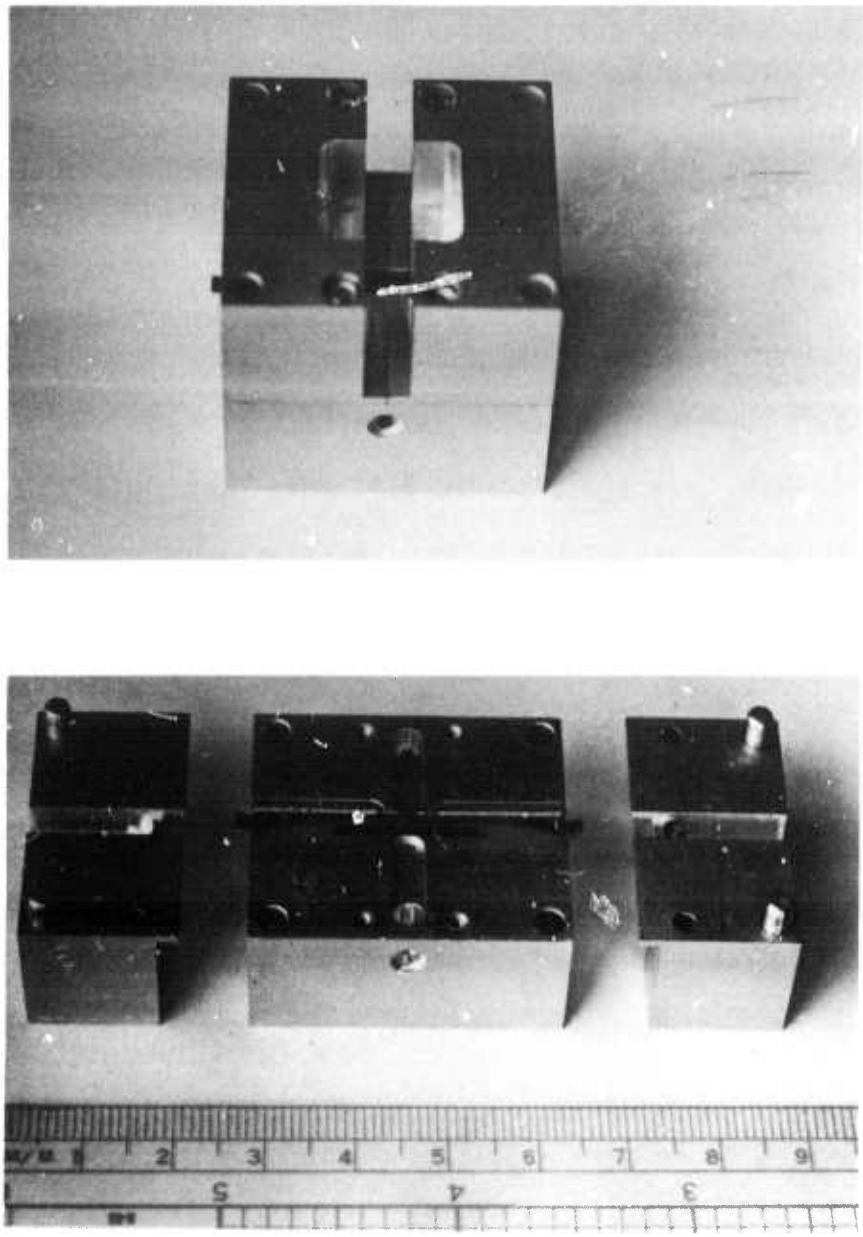


Figure 63 Assembled and disassembled photographs of the Ka-Band waveguide to microstrip which has been scaled from the TRW design at W-Band. The Duroid microstrip transition can be seen in the lower photograph.

mil thick Rogers Duroid 5880. It is anticipated that a hard substrate such as 0.010" thick quartz [34] may be used to facillitate transitions between the device under test and the microstrip line. The transition length and curvature were generated by scaling a TRW W-Band test fixture [35] down to Ka-Band. To enhance manufacturability, a simple cosine taper is used to approximate the optimum cosine series coupling distribution [36]. In order to minimize reflections from the air dielectric interface quarter wave transformers [37] have been introduced in the form of a dielectric protrusion at each end of the fixture. The finline is isolated from the housing by a thin strip of mylar tape. This allows dc bias to be introduced onto the microstrip line while effectively grounding the finline at millimeter-wave frequencies through the mylar capacitor.

The printed circuit mask was designed on the GDS II CALMA computer aided design system. The tape output from the CALMA station was used to produce top and bottom glass masks on a Mann pattern generator. The glass masks were found to be incompatible with the etching facilities at hand, so the patterns were transferred to Kodak mylar Precision Line Film with a collimated beam of light. The top and bottom mylar masks were then aligned to within 2 mils and taped together with 7 mil thick double sided tape (Fig. 64).

The printed circuits were fabricated using standard photolithographic techniques. The Duroid boards were spin coated with Shipley 340B resist and exposed with a collimated 400 W light beam for 2.5 minutes in a Cannon Contact mask aligner. Microposit 303A developer was then used, followed by etching in a ferric chloride solution. After

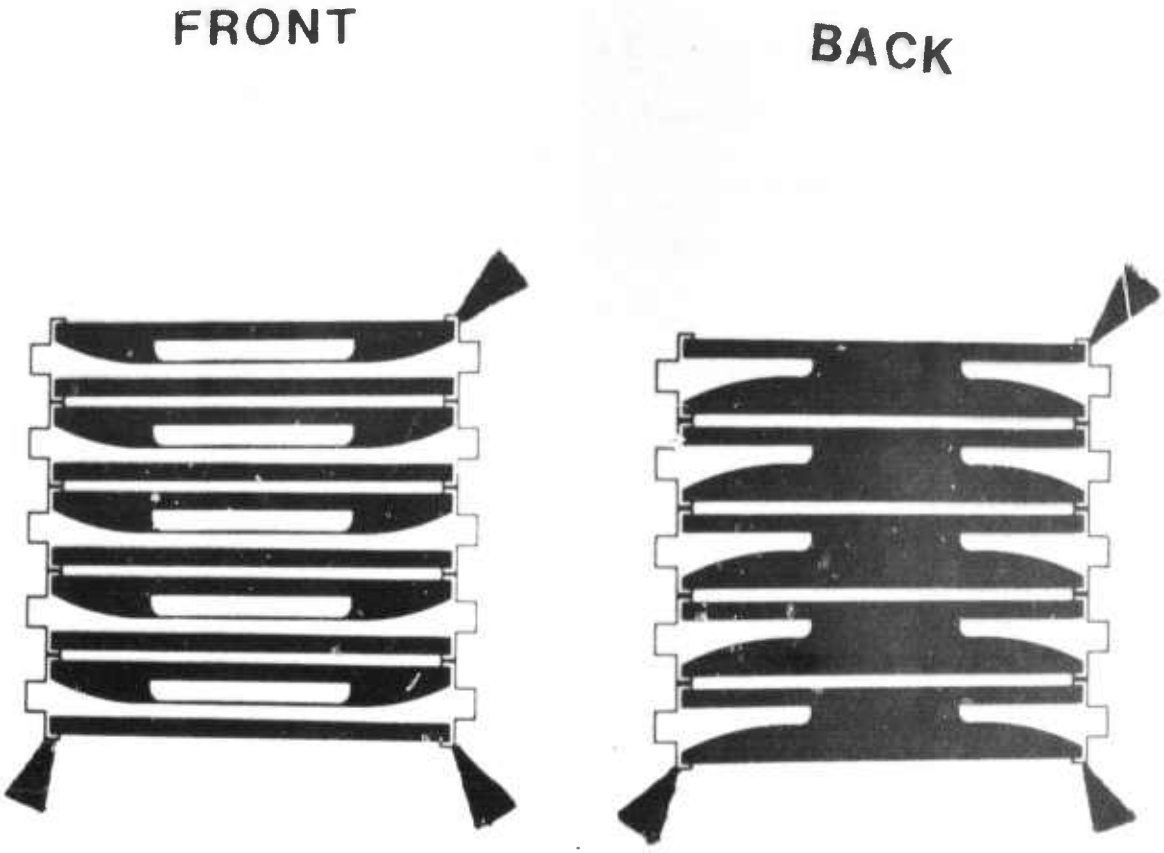


Figure 64 The top and bottom mylar masks that are used to pattern the microstrip transition onto the Duroid.

gold plating per MIL-G-45204 50 micro-inches minimum, the boards were ultrasonically cleaned and trimmed to size by hand for assembly into the fixture.

Two housings were machined out of soft brass, requiring ten hours of machinist time including the time to program the computer controlled Bridgeport milling machine. In retrospect there are several tight tolerances and machine steps that may be eliminated, which would allow the housings to be produced at substantial savings over the prototype version. The housings were gold plated per MIL-G-45204 50 micro-inches minimum and ultrasonically cleaned before assembly.

Performed on the computer-aided four port network analyzer developed on this contract. The sophisticated computer program provided the data illustrated in Fig. 65. Insertion loss was measured with a waveguide short at Port 2 of the test fixture while a load with better than 1.2:1 VSWR was used for the reflection measurement. The network analyzer has an accuracy that has been demonstrated to be better than 0.2 dB.

Figure 66 is the swept frequency data for the test fixture. The VSWR is 1.3:1 at the design frequency of 36 GHz, and is better than 1.8:1 from 26.5 to 36.8 GHz. The fixture is currently being experimentally optimized to improve the VSWR from 36.8 to 40 GHz and reduce the insertion loss over the entire band. The poor VSWR above 36.5 GHz is thought to be due to parastic resonances. An additional metallization, if added properly to the circuit, can prevent the metal-free region below the tapes from resonating within the Ka-Band.

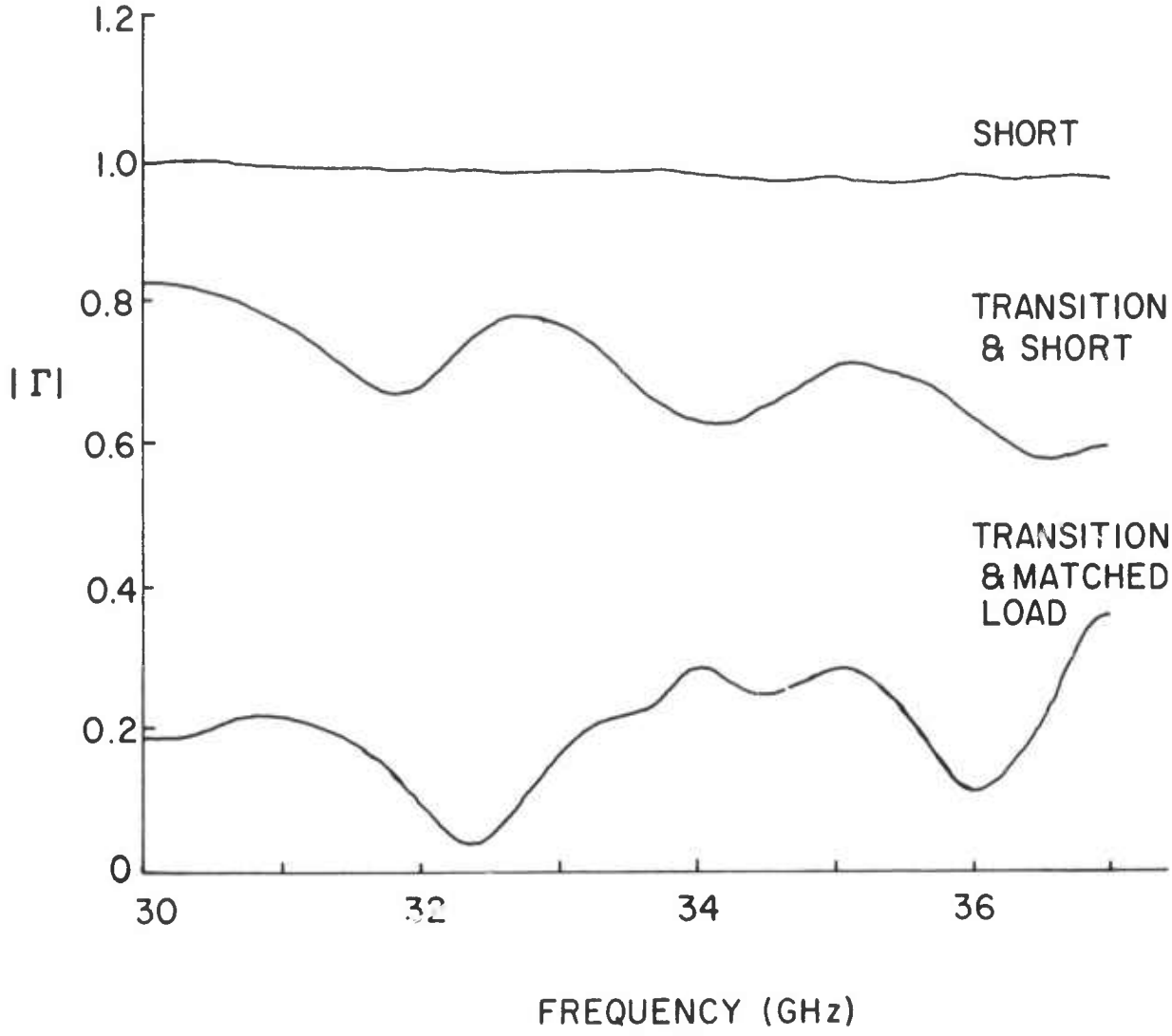


Figure 65 Reflection coefficient data obtained from the network analyzer for the waveguide-microstrip transition with the second port terminated in a waveguide short.

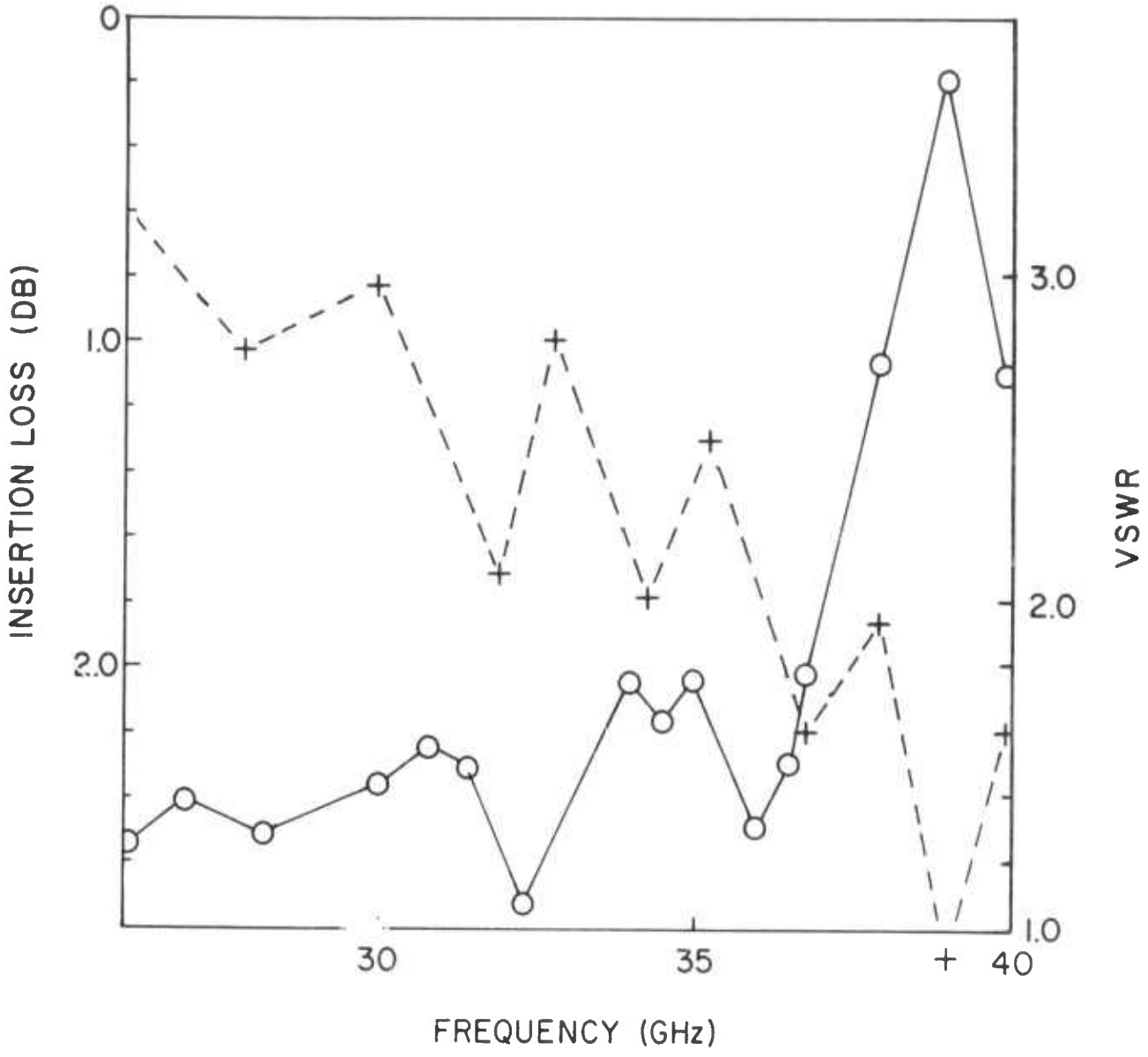


Figure 66 The test fixture VSWR as a function of frequency.

With good VSWR and reasonable insertion loss this test fixture will be ideal for use in the development of millimeter-wave devices and circuits.

2.3.3 Small Transmission Line Interconnects (G. C. Dalman, A. Yarborough)

Since the physical size of the transistor to be tested is very small, suitably designed transmission lines are required which taper from the small transistor device up to the relatively large dimensions of the microstrip section of the waveguide-microstrip adaptor. Work (partially sponsored by the Semiconductor Research Corporation (SRC)) is under way to fabricate suitable structures. Progress made to date is as follows:

a. Polyimide has been shown to be a suitable dielectric substrate for very small microstrip transmission lines.

b. A simple transmission resonator test structure has been developed to evaluate the losses in microstrip lines.

c. Several experimental lithography techniques have been developed for fabricating small microstrips.

d. A new trench waveguide structure, shown in Fig. 67, is being evaluated for millimeter-wave work.

2.3.4 Microwave Measurements on OGST's (K. Rauschenbach, J. Bellantoni, and C. A. Lee)

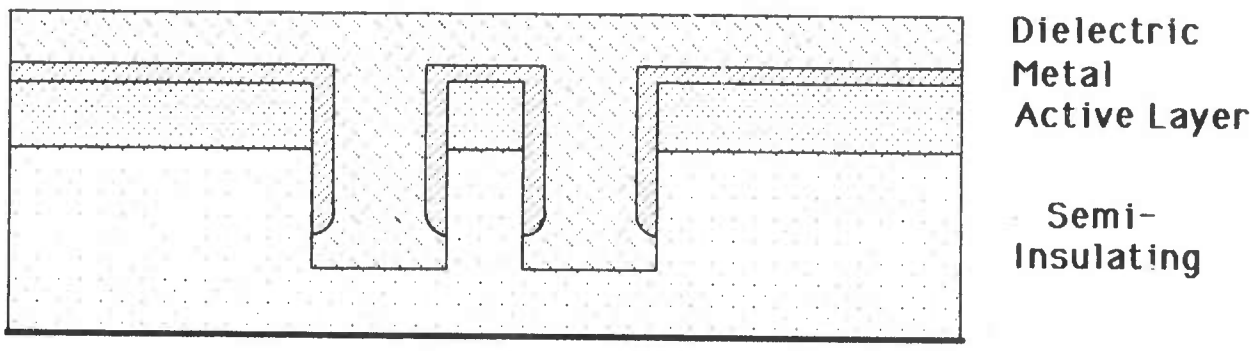
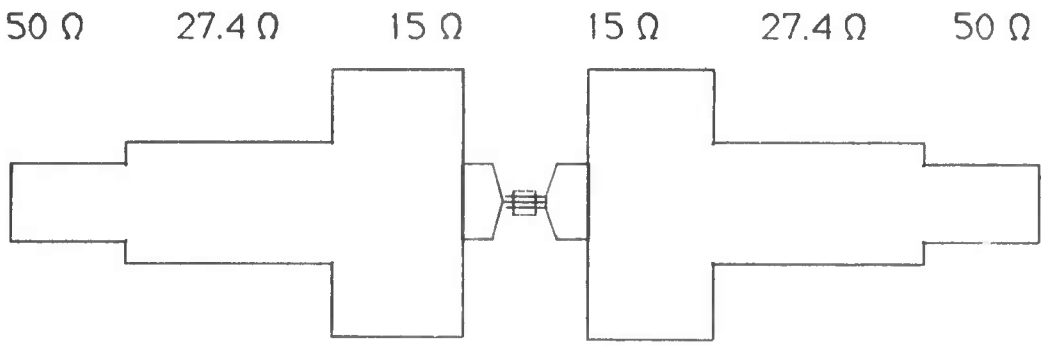


Figure 67 A schematic cross section of a new "trench" waveguide being evaluated for millimeter-wave work.

The transistors described in Section 2.1.3 were mounted in a Duroid test fixture for S parameter measurements up to 18 GHz in an HP 8510 Network Analyzer. The Duroid 5880 microstrip fixture is shown schematically in Fig. 68. The 27.4 Ω sections represent quarter wave transformers to match the transistor input and output lines at 18 GHz. Figure 69 shows a photograph of the fixture containing the Duroid circuit and a mounted transistor. Figure 70 shows a magnified view of an OGST mounted in the Duroid circuit.

Although some half dozen transistors were mounted and tested the microwave tests were largely unsuccessful. A sample of the microwave data is shown in Fig. 71 which shows no indication of transmission gain. This result was disappointing in view of the fact that probe measurements had indicated oscillations and reasonable transconductances had been measured. Microscopic examination of the transistors after mounting revealed that many of the gate electrodes were detaching themselves from the active layer. It seems that flexure of the 75 μm GaAs substrate although it was insufficient to break the membrane it was sufficient to make the gates curl up away from the membrane. This adhesion problem had arisen earlier when deposition stress in the tungsten metallization became too great. By manipulating the conditions of deposition this stress could be reduced to very low values, but the flexure encountered in mounting is evidently too great to maintain adhesion. A layer of titanium would improve the adhesion, but there was not time to redo those metallizations. Effort will continue to mount a transistor for microwave measurement.



Microstrip Circuit for Embedding OGST

Figure 68 Microstrip fixture of Duroid 5880 for embedding OGST for network analyzer measurements.

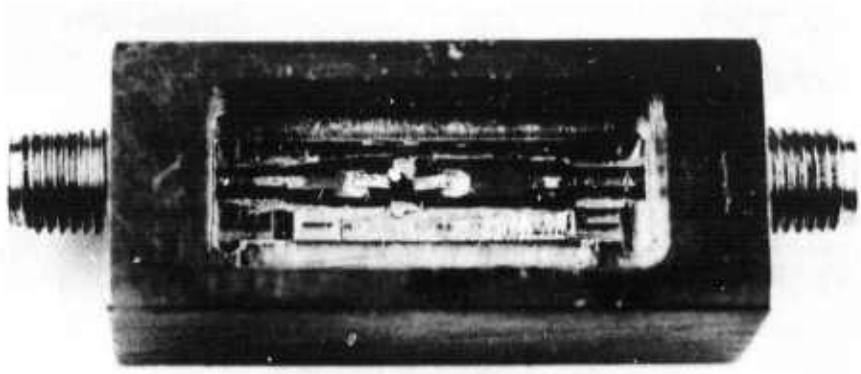


Figure 69 Photograph of fixture containing Duroid microstrip fixture and a mounted transistor.

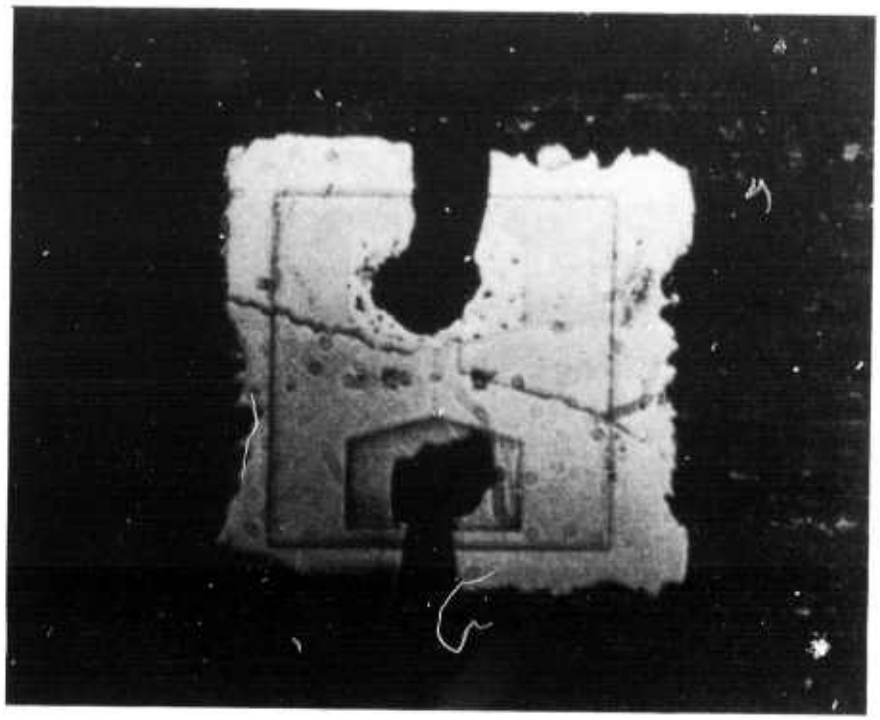


Figure 70 Magnified view of an OGST mounted in the Duroid microstrip fixture.

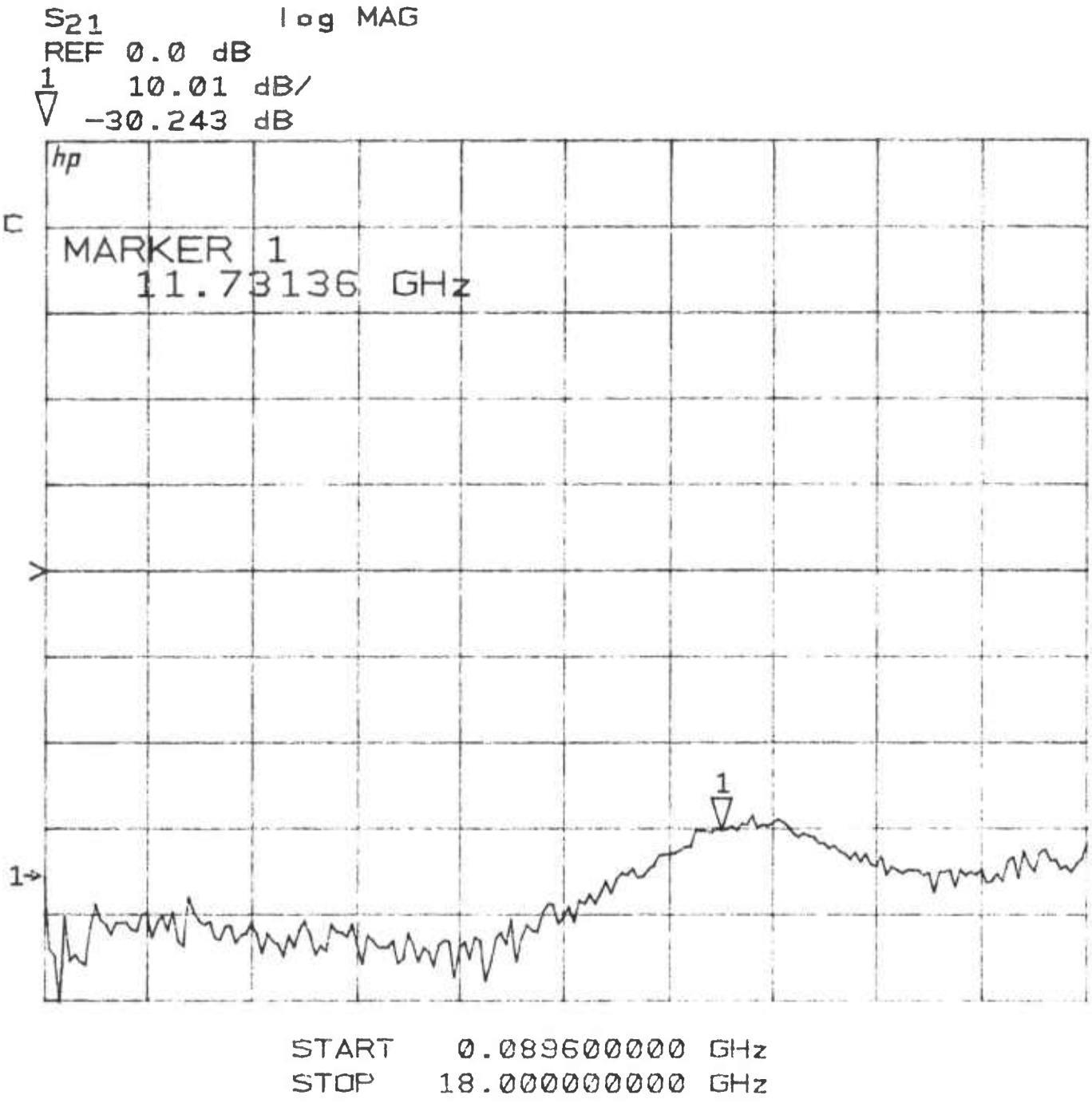


Figure 71 Unsuccesful measurement of S_{21} of a mounted OGST.

REFERENCES

[1] S. Tiwari, T. Kuan, and E. Tierney, "Ohmic Contacts to n-GaAs With Germanide Overlayers,"International Electron Devices Meeting, IEEE, Washington DC, Dec. 1983, p115.

[2] A. Iliadis and K. E. Singer, "The Role of Germanium in Evaporated Au-Ge Ohmic Contacts to GaAs," Solid-State Electronics, Vol. 26, No. 1, pp 7-14, 1983.
W. E. Stanchina and J. E. Whelan, "Solubility of GaAs in Au-Ge Eutectic Melts," Solid-State Electronics, Vol. 26, No. 8, pp. 817-819, 1983.

[3] J. Nulman and J.P. Krusius, "Local Plasma Oxidation and Reactive Ion Etching for Ultra Fine Line Pattern Inversion and Transfer", J. Vac. Sci. Technol. B1 (1983)1033-1036.

[4] J.P. Krusius, J. Nulman, and A. Perera, Self-Aligned Dual Surface Lithography, J. Vac. Sci. Technol. B4(1) 1986, 360-374.

[5] BDT-510 is a product and trade mark of SEL-REX.

[6] J. Nulman and J.P. Krusius, Novel Fine Line Pattern Technique for Submicron Devices Based on Selective Oxidation of Aluminum, Applied Physics Letters 42, p. 442, 1983.

[7] M. L. Schattenburg, I. Plotnik, and Henry I. Smith, "Reactive-Ion Etching of 0.2 μm Period Gratings in Tungsten and Molybdenum Using $CBrF_3$," J. of Vacuum Science and Technology B3 (1), Jan/Feb 1985.

[8] W. G. Oldham and E. Hieke, "A High Resolution Negative Electron Resist by Image Reversal," IEEE Elec. Dev. Lttr., EDL-1, No. 10 Oct. 1980.
T. D. Berker and D. D. Casey, "Characterization of AZ-2415 as a Negative Electron Resist," IEEE Trans. on Elec. Dev., Vol. ED-29, pp. 524-530, No. 4, April 1982.

[9] E. D. Palik, Ed , "Handbook of Optical Constants of Solids," Academic Press, 1985.

[10] X. S. Wu, L. A. Coldren and J. L. Merz, "Selective Etching Characteristics of HF for $Al_xGa_{1-x}As$," Electronics Lttrs., Vol. 21, No. 13, 2 June 1985.

[11] Kevin C. Lee, J. Silcox, and C. A. Lee, "Schottky Barrier Diode on a Submicron Thick Silicon Membrane Using A Dual Surface Fabrication Technique." J. Appl. Phys., Comm., Dec. 1, 1986.

[12] See e.g. K. Murata, D. Kyser, and C. Ting, J. Appl. Phys. 52(1981)4396.

[13] A modified version of EXPOL has been used here. EXPOL originates from I. Adesida. A deescription of the underlying physics is given

in N. Samoto, R. Shimizu, H. Hashimoto, I. Adesida, and E. Wolf, J. Vac. Sci. Technol. B1(1983) 1367.

[14] R.E. Jewett, P.I. Hagouel, A.R. Neureuther, and T. Van Duzer, Poly. Eng. Sci. 17 (1977) 381.

[15] M. Hatzakis, C.H. Ting, and N. Viswanathan, Proc. 6th Int. Conf. Electron and Ion Beam Science and Technology, edited by R. Bakish (The Electrochemical Society, Princeton, 1974), p.542.

[16] A.R. Neureuther, D.F. Kyser, and C.H. Ting, IEEE Trans. Electron Devices ES-26(1979) 686.

[17] A modified version of TRIM was used here. TRIM originates from J. Biersack, Hahn-Meitner Institute, Berlin, Germany. For a description see J.P. Biersack, and L.G. Haggmark, Nucl. Instruments and Measurements 174(1980)257.

[18] See e.g. E. Spiller and R. Feder, X-Ray Lithography, in H.J. Queisser (ed.) X-Ray Optics (Springer Verlag, New York, 1977).

[19] For a definition of these quatities see e.g. D.A. McGillis, Lithography, in S.M. Sze (ed.) VLSI Technology (McGraw-Hill, New York 1983).

[20] N.D. Wittels, Fundamentals of Electron and X-Ray Lithography, in R. Newman (ed.) Fine Line Lithography (North-Holland, New York, 1980).

[21] H. Betz, K. Heinrich, A. Heuberger, H. Huber, and H. Oertel, J. Vac. Sci. Technol. B4(1), 248-252, 1986.

[22] J.V.Faracelli, J.Frey, J.P.Krusius, "Physical basis for Short Channel MESFET operation II: Transient behaviour, IEEE Trans. Electron Devices, **ED-20**,p.377,1982.

[23] D.L.Scharfetter, H.K.Gummel, "Large signal analysis of silicon Read diode", Trans. Electron Devices, **ED-16**,p.64,1972.

[24] A. Jennings, Matrix Computations for Engineers and Scientists. New York; John Wiley,1977.

[25] M.Reiser, "Large signal numerical simulation in semiconductor device modelling", Comput. Methods Appl. Mech. and Eng., vol.1,p.17,1972.

[26] P. Krusius and J.J. Berenz, "Simulation and Performance of the Novel High Frequency FET with an Opposed Gate Source Structure", IEEE Trans. Electron Devices, **ED-30**, #9, pp.1116-1122.

[27] T.C. Edwards, "Foundations for Microstrip Circuit Design", J. Wiley, 1983.

[28] K.C. Gupta, R. Garg, and R. Chadha, Computer Aided Design of Microwave Circuits, Artech House, 1985.

[29] W. Jutzi, Uniform Distributed Amplifier Analysis with Fast and Slow Waves, Proceedings of IEEE 56, pp. 66-67, 1968.

[30] Y-C Wang and M. Bahrami, Distributed Effects in GaAs MESFET, Solid State Electronics, 22, pp. 1005-1009, 1979.

[31] G. W. McIver, "A Traveling Wave Transistor," IEEE Proc., Vol. 53, pp. 1747-1748, Nov. 1965.

[32] A. Perera, J.P. Krusius, C.A. Lee, and G.C. Dalman, "Symmetry, Transient, and Distributed Characteristics of Opposed Gate Source Transistor', manuscript to be submitted for publication in August 1986.

[33] J. H. C. van Hevven, "A New Integrated Waveguide-Microstr[illegible] Transition," IEEE MTT-24, pp 144-146, Mar 1976.

[34] Sholley, Mass, Allen et al, "HEMT mm-Wave Amplifiers, Mixers, and Oscillators," Microwave Journal, pp 120-130, August 1985.

[35] TRW test fixture supplied by Dr. Cheng Sun.

[36] C. S. Schieblich, J. K. Piotrowski, and J. H. Hinten, "Synthesis of Optimum Finline Tapers Using Dispersion Formulas for Arbitrary Slot Widths and Locations," IEEE MTT-32, pp 1634-1644, December 1984.

[37] C. S. Verves, . J. Hoefes, "Quarterwave Matching of Waveguide to Finline Transitions," IEEE MTT-32, pp 1645-1648, Dec. 1984.

[38] H. Kondoh, G. C. Dalman, "A New Computer-Aided Four Port Vector Network Analyzer for Millimeter-Wave Frequencies," Cornell University School of Electrical Engineering (Appendix I).

[39] G. Begemann, "An X-Band Balanced Finline Mixer," IEEE MTT-2[illegible], pp 1007-1011, Dec. 1978.

Appendix I. Process Schedule for Demonstration of Dual Surface X-Ray Lithography
(J.P. Krusius, J. Hulman, and A. Perera)

Starting Material	: Silicon
Structure	: n-type, 0.92 - 0.96 ohm-cm, (100)
Source	: Silicon Processing Co. Boston, MA.
Thickness	: 12 +/- 1 mils

(1) Cleaning process No. 1

(2) Boron deposition

Source	: solid BN disks
Vendor	: The Carborundum Co.
Grade	: BN-975
Lot No.	: 8501
Size	: 3" dia. X 0.040"

Boron Nitride diffusion source disk preparation

Clean	: Acetone 3 min
Rinse	: DI H_2O 5 min
Clean	: Buffered SiO_2 etch 4 min
Rinse	: DI H_2O 5 min
Blow-dry	: Nitrogen

Thermal cycle

System	: Thermco, TCA tube
Temperature	: 950 °C
Time	: 25 min, dry O_2
	45 min, dry N_2

Deposition

System	: Thermco
Temperture	: 1150 °C
Time	: 45 min
Thickness	: 3-2 μm

(3) Initial Cleaning Process

Bath No.1	: Methyl Chloride (CH_3Cl) 1 min
Bath No.2	: Methyl Alcohol 30 sec
	N_2 blow-off
Spin rinse	: Acetone 1 min
	Methyl Alcohol 1 min
	DI water 1 min
Bath No.3	: Hydro-flouric acid 49% 15 sec
	DI H_2O_2 30 sec
	N_2 blow-off

(4) Deposition of electroplating base (Cr-Au)

Thermal Evaporation of Chrome

System	: CHA
Base pressure	: 4.0×10^{-7} torr
Tooling	: 140.0 %
Source	: chrome plated W rod (source No. 3)
Chrome Vendor	: R. D. Mathis Company
Power	: 65 A/ 10 V
Thickness	: 50 Å
Thickness (actual)	: 50 Å ±2.0 %

Rate : 1.5 Å/sec

Thermal Evaporation of Gold

System : CHA

Base Pressure : 4.0×10^{-7}

Tooling : 126.0 %

Source : Gold chips in ceramic boat (source no.2)

Gold Vendour : The Mine

Power : 27 A/ 10 V

Thickness : 200 Å

Thickness (actual) : 200 Å ±2.0 %

Rate : 2.5 Å/sec

(5) Standard Clean

Spin Rinse : Acetone 1 min

Methonol 1 min

DI H_2O 1 min

Bake : 170 °C, atmosphere, 1 hour

(6) Tri - Layer Resist Deposition

Polyimide spin on

Vendor : CIBA-Geigy Corparation

Model : XU284

Spin Speed : 5000 rpm

Time : 120 sec

Cure : 170 °C, atmosphere, 1 hour

250 °C, N_2 ambient, 1 hour

Thickness : 8500 Å 15%

Plasma depositon of SiO_2

System : Technics

Base Pressure : < 0.1 mTorr

Deposition pressure : 435 mTorr

Temperature : 200 °C

Power : 37 Watts

N_2O flow rate : 60 sccm (109 mm)

SiH_4 flow rate : 6 sccm (partial pressure = 64 mTorr)

Deposition rate : 425 Å/min

Time : 1 min 25 sec

Thickness : 650 Å

Pmma spin on

Vendour : KTI Chemicals Inc.

Dilution : 4 % in chloro-benzene

Speed : 6000 rpm

Time : 60 sec

Post-Bake : 170 °C, atmosphere, 1 hour

(7) Electron beam Lithography of gate level of ring oscillator and sets of lines

System : Cambridge Instruments, EBMF6

Beam Current : 2 nA

EHT : 30 KEV

Clock rates (≥ 1 μm) : 200 KHz

(0.3 μm) : 70 KHz, 1 pass lines

(0.4 μm) : 63 KHz, " "

(0.5 μm) : 56 KHz, " "

Field size : 3.2 mm

Field size calibration : manual

Distortion corrections : off

Focussing : manual

Aperture : No. 2, 400 μm

Development of electron beam exposure

Developer : MIBK:IPA (Methyl Iso-Butyl Ketone: Iso-propyl alcohol) 1:1

Time : 2 min

Temperature : room temperature

Agitation : yes

Rinse : IPA at RT, 30 sec
flowing DI at RT, 30 sec
N_2 blow-off

(8) Pattern the SiO_2 and polyimide

E-beam resist descum

System : Applied Materials

Base pressure : 5×10^{-5} Torr

Etch pressure : 30 mTorr

Electrode : quartz

Gas : oxygen (O_2)

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

DC Bais : -440 V

Time : 15 sec

Reactive Ion Etch of PECVD SiO_2

Gas : Freon 23 (CHF_3)

Etch pressure : 30 mTorr

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

DC Bias : -360 V

Time : 6 min

Reactive Ion Etch of Polyimide

Gas : oxygen (O_2)

Etch Pressure : 30 mTorr

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

DC Bias : -440 V

Time : 8 min

(9) Gold Electro-plating of gate features

Electrolyte : BDT-510

Vendor : Sel Rex Co.

Temperature : 50 °C

Stirring : 2.5 on Cole Parmer hotplate no.4812

Current : 125 μA

Anode : Platinum

Vendor : Sel Rex Co.

Plating rate : 2000 Å/min

(net plating area = 1 cm^2)

Time : 4 min

Thickness : 8000 Å ± 6%

(10) Tri layer resist removal (RIE)

Pre-etch clean

System	: Applied Materials
Base pressure	: 5×10^{-6}
Gas	: oxygen (O_2)
Etch pressure	: 30 mTorr
Electrode	: quartz
Flow Rate	: 30 sccm
Power	: 0.25 Wcm^{-2}
Bais	: -440 V
Time	: 2 min

PECVD SiO_2 Etch

Gas	: Freon 23 (CHF_3)
Etch pressure	: 30 mTorr
Flow Rate	: 30 sccm
Power	: 0.25 Wcm^{-2}
Bias	: -370 V
Time	: 10 min

Polyimide removal

Gas	: oxygen
Etch pressure	: 30 mTorr
Flow rate	: 30 sccm
Power	: 0.25 Wcm^{-2}
Bias	: -440 V
Time	: 10 min

(11) Ion Milling of plating base

System	: Millatron
Gas	: Argon
Base Pressure	: 4×10^{-6} Torr
Chamber pressure	: 2×10^{-5} Torr
Gun pressure	: 2×10^{-4} Torr
Cathode	: 11.5 V, 15 A
Magnet	: 3.0 V, 2.5 A
Accelerator	: 500 V
Extractor	: 350 V
Stage rotation	: on
Beam current	: 38 mA
Etch time	: 40 sec

(12) Photolithography (membrane area definition)

Dehydradation bake	: 1 hour at 150 °C, in air ambient
Primer coating	: Microposit C-30
	set for 15 sec,
	spin at 5000 rpm, 30 sec
Resist coating	: AZ-1350J
	spun at 3000 rpm, 30 sec
	$\simeq$ 2μm thick
Softbake	: 80 °C, 15 min, air ambient
Exposure	: Cobilt 400A Proximity Aligner
	flood exposure, 45 sec
	intensity = 5 $mWcm^{-2}$
Developement	: 2 min, 30 sec, Shipley 606 developer

Rinse	: 2 min in flowing DI water
Spin dry	: 5000 rpm, 30 sec
Postbake	: 10 min, 90 °C, air ambient

(13) Membrane etch mask (back surface Si_3N_4) patterning

Etchant	: Buffered SiO_2 etch
	Ammonium Fluoride 40% solution:HF acid, 6:1
Time	: 34 min
Rinse	: 5 min in DI
Blow dry	: Nitrogen

(14) Membrane etch

Etchant	: 40 gm Catechol
	250 ml Ethyldiamene
	160 ml DI H_2O
Temperature	: 70 °C
Time	: 12 hours
Rinse	: 10 min in DI H_2O
Blow-off	: Nitrogen (VERY gently)

(15) Dual-surface X-ray lithography

Dehydradation bake	: 1 hour, 170 °C, air ambient
Resist coating	: PMMA, 4% solution in Chlorobenzene
	4000 rpm, 60 sec
Postbake	: 1 hour, 170 °C, air ambient
Exposure	

System	: home grown
Target	: Copper
Wavelength	: 13.336 Å ($Cu_{L\alpha}$)
Power	: 0.75 KW
Filter	: Infra Red - 1 μm Polyimide (duPoint PI-2555), 1000 Å Aluminium
Time	: 22 hours
Developement	: MIBK:IPA 1:1, at RT, 2 min 30 sec
Rinse	: IPA, at RT, 30 sec
	DI H_2O, at RT, 30 sec
Dry	: Air flow of hood

(16) Plasma deposition of Si_3N_4 and liftoff

(17) Source metal (Au:Ge) deposition

Appendix II. Process Schedule for OGST Fabrication with Dual Surface X-Ray Lithography

(J.P. Krusius, J. Hulman, and A. Perera)

Starting Material

Structure : 2000 Å nGaAs/150 Å AlGaAs MBE layers on a semi insulating GaAs substrate

Source : T.R.W.

Thickness : 9 - 12 mils

(18) Initial Cleaning Process

Bath No.1 : Methyl Chloride (CH_3Cl) 1 min

Bath No.2 : Methyl Alcohol 30 sec

N_2 blow-off

Spin rinse : Acetone 1 min

Methyl Alcohol 1 min

DI water 1 min

Bath No.3 : Hydro-flouric acid 49% 15 sec

DI H_2O_2 30 sec

N_2 blow-ff

(19) Sputter Deposition of Schottky Gate (TiW)

System : CVC

Base pressure : 2.3×10^{-7} Torr

Pre Sputtering

Substrate Bias : 100 W

Target : TiW, No. 3

DC Mag. : 2.0 KW, 571 V, 3.5 A

Control mode = Amps

Sputtering gas : Argon/N_2 (5%)

flow rate = 40/2 sccm

Sputtering pressure : 10 mTorr

Substrate rotation : 4

Shutter position : closed

Back sputter time : 10 min

Throttle : 0.755

Bias Etch

last one minute of pre-sputter

Film deposition

Substrate Bias : 100 W

DC Mag. : 2.0 KW, 571 V,3.5 A

Control mode = Amps

continued from previous step

Sputtering gas : Argon/N_2 (5%)

Sputtering pressure : 10 mTorr

Substrate rotation : 4

Shutter position : open

Deposition time : 10 min

Thickness (desired) : 2000 Å (unannealed)

Thickness (actual) : unknown Å (unannealed)

(20) Evaporation of Chrome

System	: CHA
Base pressure	: 4.0×10^{-7} torr
Tooling	: 140.0 %
Source	: chrome plated W rod (source No. 3)
Chrome Vendor	: R. D. Mathis Company
Power	: 65 A/ 10 V
Thickness	: 50 Å
Thickness (actual)	: 50 Å ±2.0 %
Rate	: 1.5 Å/sec

(21) Evaporation of Gold

System	: CHA
Base Pressure	: 4.0×10^{-7}
Tooling	: 126.0 %
Source	: Gold chips in ceramic boat (source no.2)
Gold Vendour	: Cominco
Boat Vendor	: Sylvania
Power	: 27 A/ 10 V
Thickness	: 200 Å
Thickness (actual)	: 200 Å ±2.0 %
Rate	: 2.5 Å/sec

(22) Standard Clean

Spin Rinse	: Acetone 1 min
	Methonol 1 min
	DI H_2O 1 min
Bake	: 170 °C, atmosphere, 1 hour

(23) Tri - Layer Resist Deposition

Polyimide spin on

Vendor	: CIBA-Geigy Corparation
Model	: XU284
Spin Speed	: 5000 rpm
Time	: 120 sec
Cure	: 170 °C, atmosphere, 1 hour
	250 °C, H_2 ambient, 1 hour
Thickness	: 8500 Å ± 15%

Plasma depositon of SiO_2

System	: Technics
Base Pressure	: < 0.1 mTorr
Deposition pressure	: 435 mTorr
Temperature	: 200 °C
Power	: 37 Watts
N_2O flow rate	: 60 sccm (109 mm)
SiH_4 flow rate	: 6 sccm (partial pressure = 64 mTorr)
Deposition rate	: 425 Å/min
Time	: 1 min 25 sec
Thickness	: 650 Å

Pmma spin on

Vendour	: KTI Chemicals Inc.
Dilution	: 4 % in chloro-benzene
Speed	: 6000 rpm
Time	: 60 sec
Post-Bake	: 170 °C, atmosphere, 1 hour

(24) Electron beam Lithography of Gate Level

System : Cambridge Instruments, EBMF6

Beam Current : 2 nA

EHT : 20 KEV

Clock rates (> 1 μm) : 350 KHz, gross features

(0.3 μm) : 280 KHz, 4 pass lines

(0.4 μm) : 260 KHz, " "

(0.5 μm) : 235 KHz, " "

Filename : APOGST1

Field size : 3.2 mm

Field size calibration : manual

Distortion corrections : off

Focussing : manual

Aperture : No. 2

Development of electron beam exposure

Developer : MIBK:IPA (Methyl Iso-Butyl Ketone:Iso-propyl alcohol) 1:1

Time : 1 min, 30 sec

Temperature : room temperature

Agitation : yes

Rinse : IPA at RT, 30 sec

flowing DI at RT, 30 sec

N_2O blow-off

(25) Pattern the SiO_2 and polyimide

E-beam resist descum

System : Applied MAterials

Base pressure : 5 X 10^{-5} Torr

Etch pressure : 30 mTorr

Electrode : quartz

Gas : oxygen (O_2)

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

DC Bais : -440 V

Time : 15 sec

Reactive Ion Etch of PECVD SiO_2

Gas : Freon 23 (CHF_3)

Etch pressure : 30 mTorr

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

DC Bias : -360 V

Time : 6 min

Reactive Ion Etch of Polyimide

Gas : oxygen (O_2)

Etch Pressure : 30 mTorr

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

DC Bias : -440 V

Time : 8 min

(26) Gold Electro-plating of gate features

Electrolyte : BDT-501

Vendor : Sel Rex Co.

Temperature	: 50 °C
Stirring	: 2.5 on Cole Parmer hotplate no.4812
Current	: 125 μA
Anode	: Platinum
Vendor	: Sel Rex Co.
Plating rate	: 2000 Å/min (net plating area = 1 cm^2)
Time	: 4 min
Thickness	: 8000 Å 6%

(27) Tri layer resist removal (RIE)

Pre-etch clean

System	: Applied Materials
Base pressure	: 5×10^{-6}
Gas	: oxygen (O_2)
Etch pressure	: 30 mTorr
Electrode	: quartz
Flow Rate	: 30 sccm
Power	: 0.25 Wcm^{-4}
Bais	: -440 V
Time	: 2 min

PECVD SiO_2 Etch

Gas	: Freon 12 (CHF_3)
Etch pressure	: 30 mTorr
Flow Rate	: 30 sccm
Power	: 0.25 Wcm^{-2}
Bias	: -370 V

Time : 10 min

Polyimide removal

Gas : oxygen

Etch pressure : 30 mTorr

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

Bias : -440 V

Time : 10 min

(28) TiW dry-etch

Pre etch clean

System : Applied Materials

Base pressure : 5×10^{-6}

Gas : oxygen

Etch pressure : 30 mTorr

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

Bais : -370 V

Time : 30 sec

TiW Reactive Ion Etch

Gas : Freon 14 (CF_4)

Etch pressure : 30 mTorr

Flow rate : 30 sccm

Power : 0.25 Wcm^{-2}

Bais : -270 V

Etch rate : $\simeq$ 110 Å/min

Time : 20 min

(29) Ion Milling of plating base

System	: Millatron
Gas	: Argon
Base Pressure	: 4×10^{-6} Torr
Chamber pressure	: 2×10^{-5} Torr
Gun pressure	: 2×10^{-4} Torr
Cathode	: 11.5 V, 15 A
Magnet	: 3.0 V, 2.5 A
Accelerator	: 500 V
Extractor	: 350 V
Stage rotation	: on
Beam current	: 38 mA
Etch time	: 40 sec

APPENDIX III

A Computer-Aided Four-Port Vector Network Analyzer for Millimeter-Wave Frequencies

Hiroshi Kondoh*
G. Conrad Dalman

Cornell University
School of Electrical Engineering
Phillips Hall
Ithaca, NY 14853

---

* Currently with Hewlett-Packard Co., Microwave Technology Division, Santa Rosa, CA 95401

Abstract

A new type of swept-frequency computer-aided network analyzer has been developed which provides a cost effective way of measuring complex reflection and transmission coefficients of test devices at millimeter-wave frequencies. A four-port structure constitutes a heart of the system the state of which is internally switched to allow six-port-like operation with fewer impedance calibration standards.

An experimental 26.5-40 GHz network analyzer has been successfully constructed. With frequency tracking error correction only, the maximum error in the measurement of reflection coefficient was found to be ±0.16 dB in magnitude and ±1.2 degrees in phase.

I. Introduction

Renewed activities in millimeter-wave research has stimulated a demand for fast, low cost, accurate and reliable equipment for the measurement of the impedance characteristics of components and devices over a wide frequency range.

Among the existing network analyzer schemes the most widely accepted are the down-converter type analyzer and the 6-port analyzer. The former allows real time measurement of complex impedance [1] but requires an initial investment of a costly commercial microwave network analyzer and a frequency down-converter section having such expensive components as a well-matched pair of wideband mixers and a highly-stabilized local oscillator. Additional computer-aided error correction is usually required if wideband operation and high accuracy are desired.

The 6-port network analyzer has been developed and widely accepted as a very accurate way of determining a complex impedance from only four power meter readings without requiring complicated direct phase measurement [2]-[7]. The scheme owes its superb accuracy basically to a postulated computer software rather than to hardware perfectness. The simplicity of the hardware configuration contributes to a significant reduction in system cost. At millimeter-wave frequencies, however, wideband power detectors such as a thermistor bridge or a diode detector are fairly expensive and can account for a considerable fraction of the hardware cost.

As an attempt to further reduce equipment cost, a modified six-port network analyzer which requires only two power detectors has been developed. The new analyzer consists physically of only four-ports but

effective six-port operation is achieved by an internal switching of the circuit state by either mechanical or electronic means.

The operating principles of the new analyzer are described in Section 2 which follows. Section 3 deals with the performance of an experimental 26.5-40 GHz network analyzer and some discussion of the accuracy of the measurements, based on the experimental results obtained, is presented in Section 4.

II. Principle of Operation

Figure 1 shows a schematic diagram of the four-port network analyzer system. Although this configuration allows for both reflection and transmission measurements, due to formulation similarity the following discussion will be centered only on the reflection measurement case.

The four ports of the system are defined as those connected to the sweeper, the device under test (DUT) and the two power detectors. Wave notation in the figure follows a six-port convention [2]. The mm-wave signal from the computer-controlled sweeper is delivered to the device under test (DUT) as b_2. This signal is monitored through the coupler c1 and provides the reference signal, V_r. A part of wave a_2, reflected from the DUT, is coupled through c2 to become test signal V_t. The two signals, V_r and V_t are combined in a magic tee and their resultants, b_3 and b_4, are detected by the two power detectors shown connected to the colinear arms of the magic tee. As for the 6-port case, a set of four power measurements is required to determine the complex reflection coefficient of the DUT. Two independent sets of power readings are obtained by internally switching the reference channel phase from 0 to 90 degrees through the use of a phase shifter inserted in the reference channel. This scheme achieves six-port-line operation with only two power detectors, rather than the four needed in the six-port system, thereby lowering the cost of system. The electronic PIN phase shifter shown in the figure can be replaced by a simple mechanically movable short if real-time operation is not essential.

The principle of operation of the 4-port network analyzer is described as follows: assuming first the ideal case in which all of mm-

wave components are perfect, the power readings on detectors 1 and 2 are as with the phase shifter in its OFF state (no phase shift added),

$$P_1 = |b_3|^2 \sim 1 + |\Gamma^2| + 2|\Gamma|\cos\theta \qquad (1)$$

$$P_2 = |b_4|^2 \sim 1 + |\Gamma^2| - 2|\Gamma|\cos\theta$$

With the phase shifter in its ON state (90° phase shift added)

$$P'_1 = |b'_3|^2 \sim 1 + |\Gamma^2| + 2|\Gamma|\sin\theta \qquad (2)$$

$$P'_2 = |b'_4|^2 \sim 1 + |\Gamma^2| - 2|\Gamma|\sin\theta$$

where Γ is the reflection coefficient of the DUT and $\Gamma = |\Gamma|e^{j\theta} = a_2/b_2$.

Equations (1) and (2) uniquely determines both $|\Gamma|$ and θ, as discussed by Somlo [8].

When the system is not ideal, the power readings on the detectors should be expressed in the following general form, which resembles the six-port set of equations [2].

With the phase shifter in its OFF state

$$P_1 = |b_3|^2 = |A|^2|b_2|^2\ |\Gamma-q_3|^2 \qquad (3)$$

$$P_2 = |b_4|^2 = |B|^2|b_2|^2\ |\Gamma-q_4|^2$$

With the phase shifter in its ON state

$$P'_1 = |b'_3|^2 = |C|^2|b'_2|^2\ |\Gamma-q'_3|^2 \qquad (4)$$

$$P'_2 = |b_4|^2 = |D|^2|b'_2|^2\ |\Gamma-q'_4|^2$$

where A, B, C, and D and q's are system parameters.

q_i's (i=1,...,4) equal to -1, +1, -j, +j respective in the ideal case.

Once the system parameters have been obtained by the system calibration, the unknown reflection coefficient, Γ, of a DUT is determined from these equations as an intersecting point of four circles in a Γ plane.

It should be noticed here that, for a given Γ, Eqs. (3) and (4) are two independent sets of equations, representing two independent system states, each of which contains seven real numbers as system parameters. Thus the system calibration for the four-port analyzer requires 3 1/2 impedance standards as a minimum. This compares favorably with the 5 1/2 required in a conventional six-port scheme. This reduction in required number of standards makes the calibration steps simpler and potentially increases its accuracy. Here the significance of a half of a calibration standard is that either the magnitude or phase of the standard must be known. For a full calibration standard, both phase and magnitude must be known.

III. Experimental 26.5-40 GHz Network Analyzer

To establish the feasibility of the proposed four-port vector network analyzer, an experimental unit was constructed for operation over a frequency range 26.5-40 GHz. Figure 2 shows the system configuration for reflection coefficient measurements.

The experimental system makes use of a mechanically movable waveguide short as a phase shifter in the reference channel. In the measurement of a DUT, one frequency sweep is made at a zero degree setting and another at a 90° setting. The frequency of the sweeper is controlled through its external FM terminal with an analog dc voltage provided by a PDP 11/40 computer. The electrical lengths of the reference and the test channels were equalized to minimize measurement errors due to frequency instability of the sweeper. Directional couplers with more than 35 dB directivity were used in the system. The DC voltage signals from the two power detectors are fed into the computer to pertorm the data processing. The results of measurement are displayed, either on a CRT or on an X-Y recorder. Printer outputs are also available.

The computer software developed for the present network analyzer system can be used for both reflection and transmission measurements and on a system operating at any frequency band of operation. The software consists of three major parts. The first part relates to the sweeper setting. The sweep frequency range is specified and then divided into 101 equally separated points. The subsequent system calibration and DUT measurements are performed at each of these frequency points. A system calibration then follows the sweeper setting. Since the principal objective of the experiment was to investigate the feasibility of the

proposed analyzer, a simplified calibration procedure was developed for the present system. Basically only frequency tracking error was taken into account in the calibration. This made the operation of the network analyzer more physically traceable. The more detailed calibration procedure can be found elsewhere [9]. The 4-port simplified system calibration requires eight frequency sweeps and takes about 15 minutes because of the slow response of the thermistors used as power detectors. The last part of the software is for the measurement routine in which the characterization of unknown DUT's and the displays of the results take place. The current software occupies 35 kBytes in memory and therefore can be accommodated easily in most personal computers.

Figure 3a shows an example of measurements in which the reflection coefficient of a waveguide short circuit was measured over a frequency range of 29 to 39 GHz. Neither phase locking nor power leveling of a sweeper has been attempted. The curves in the figure indicate both the raw data of measurement and smoothed data. The data, including its fine structure, was quite repeatable from measurement to measurement. The maximum deviation from the expected value of -1 was ± 0.5 dB in magnitude and ± 4.0 degrees in phase over the entire frequency range. The smoothing of the data was performed by taking a weighted average of data around a frequency of interest. In the present system this smoothing was found to be an effective way of reducing errors caused by the finite directivity of directional couplers, as will be discussed later. For the smoothed data the maximum deviation from a value of -1 was ± 0.16 dB in magnitude and ± 1.2 degrees in phase. Figure 3b shows the measured short data exhibited on a Smith Chart display, the unsmoothed data being shown

on the left of the figure and the smoothed data on the right.

Figure 4 shows the measured reflection coefficient of a commercial 3 dB attenuator terminated on one end by a short circuit. Also shown in Figure 4a, for comparison, are the measured points obtained using slotted line techniques. The difference between the two sets of data is ±1.1 dB maximum over a 29 to 39 GHz frequency range. Figure 4b is an unsmoothed Smith Chart display. Figure 5 shows measurements obtained on a commercial matched termination. For comparison, results obtained using slotted line techniques are also plotted in the figure. As can be seen from the figure, good agreement between the two methods of measurements was found.

An error estimation was performed for the present system [9]. Figure 6 compares the experimentally measured error with the theoretical prediction of worst-case error for reflection coefficient measurements. It should be noted that in the present system two separate mathematical algorithms were complementarily employed for solving Equations 3 and 4 in order to span a wide range of reflection coefficient values with minimum measurement errors. It was found that the accuracy of the present network analyzer system is limited mostly by the finite directivity of the directional couplers when measuring small reflection coefficients and by calibration error when measuring large values of reflection coefficients.

We believe that the effectiveness of data smoothing, clearly seen in the figures, is because the relative phases of undesirable error signals, with respect to the reference signal change rapidly with frequency and therefore can be cancelled readily out by the smoothing technique.

The undesirable error signals are mainly due to the finite directivity of the couplers and their rapid phase change results from a large difference between their path lengths and that of the reference signal.

The practical usefulness of the four-port network analyzer is demonstrated in the example shown in Fig. 7. The measured properties of an iris-coupled waveguide cavity are shown near its resonance at 34.99 GHz. Fig. 7a is a phase and magnitude plot of the reflection coefficient and Fig. 7b shows its plot on a Smith chart.

IV. Summary and Conclusion

A computer-aided four-port vector network analyzer has been developed which provides a cost effective way of measuring complex reflection and transmission coefficients of test devices at millimeter-wave frequencies on a swept frequency basis. The internal switching of the four-port circuit state by means of a 90° phase shifter yields an effective six-port operation. We believe that the four-port configuration requires a smaller number of millimeter-wave components than the six-port counterparts, leading to lower hardware cost. More importantly the four-port scheme requires only 3 1/2 impedance standards for the system calibration, compared to 5 1/2 in a six-port scheme.

An experimental computer-aided four-port vector network analyzer was constructed for 26.5-40 GHz operation. The computer linkage to the system enabled fast data processing with enhancement of accuracy. The software developed for the analyzer requires only a 35 kByte memory and is readily accommodated in most personal computers. By using a simplified system calibration procedure which takes into account only the frequency tracking error, an accuracy of ± 0.5 dB in magnitude and ± 4.0 degrees in phase was demonstrated in a test of the reflection coefficient of a waveguide short. A smoothing technique employed improved the accuracy to ± 0.16 dB and ± 1.2 degrees.

The finite directivity of directional couplers predominantly limits the accuracy of the present system. The use of a complete calibration scheme could definitely enhance the accuracy of the system. The measurement speed of the present vector network analyzer system is limited by a mechanical phase shifter and slow response of thermistors used as

power detectors.

To reduce the calibration and measurement time, studies are under way on the use of Schottky barrier diodes as power detectors in place of thermistors. Also, a 75-110 GHz version of the four-port analyzer is being assembled and the development of a PIN phase shifter is planned to achieve quasi-real-time display of measured results.

Acknowledgement

This work was supported by the Defense Advanced Research Agencies and is monitored by the Naval Ocean Systems Center under Contract No. N66001-83-C-0363.

References

[1] G.M. Yamaguchi, L.T. Yuan, and J.E. Raue, "A V-band Network Analyzer/Reflection Test Unit", IEEE Trans. Instrum. Meas., Vol. IM-25, No. 4, pp. 424-431, Dec. 1976.

[2] Glenn F. Engen, "The Six-Port Reflectometer: An Alternative Network Analyzer", IEEE Trans. Microwave Theory Tech., Vol. MTT-25, No. 12, pp. 1075-1080, Dec. 1977.

[3] G.F. Engen, "An Improved Circuit for Implementing the Six-Port Technique of Microwave Measurements", IEEE Trans. Microwave Theory Tech., Vol. MTT-25, Vol. 12, pp. 1080-1083, Dec. 1977.

[4] G.F. Engen, "Calibrating the Six-Port Reflectometer by Means of Sliding Terminations", IEEE Microwave Theory Tech., Vol. MTT-26, No. 12, pp. 951-957, Dec. 1978.

[5] C.A. Hoer, "A Network Analyzer Incorporating Two Six-Port Reflectometers", IEEE Trans. Microwave Theory Tech., Vol. MTT-25, No. 12, pp. 1070-1074, Dec. 1977.

[6] H.M. Cronson and L. Susman, "A Six-Port Automatic Network Analyzer", IEEE Trans. Microwave Theory Tech., Vol. MTT-25, No. 12, pp. 1086-1091, Dec. 1977.

[7] P.I. Somlo and J.D. Hunter, "A Six-Port Reflectometer and its Complete Characterization by Convenient Calibration Procedures", IEEE Trans. Microwave Theory Tech., Vol. MTT-30, No. 2, pp. 186-192, Feb. 1982.

[8] P.I. Somlo, "The Locating Reflectometer", IEEE Trans. Microwave Theory Tech., Vol. MTT-20, No. 2, pp. 105-112, Feb. 1972.

[9] H. Kondoh and G.C. Dalman, Cornell Internal Report, August 1984.

Figure Captions

Figure 1 Schematic diagram of a new computer-aided four-port vector network analyzer for millimeter-wave frequencies. The microwave switch is shown positioned for reflection coefficient measurement.

Figure 2 Experimental setup of a 26.5-40 GHz four-port vector network analyzer for reflection coefficient measurements.

Figure 3 Reflection coefficient measurement on a waveguide short over a frequency range of 29-39 GHz. (a) Magnitude and phase as a function of frequency. (b) Smith chart displays of the waveguide short.

Figure 4 Reflection coefficient measurements of a commercial 3 dB attenuator terminated on one end with a short circuit. (a) Magnitude of the reflection coefficient vs. frequency. The plus marks indicate measured points obtained using slotted line technique. (b) A Smith chart display in a frequency range of 29-39 GHz (unsmoothed).

Figure 5 An experimental result of a reflection coefficient measurement obtained from a commercial matched termination.

Figure 6 Comparison of experimental measurement errors with theoretical error estimates, in magnitude, for a reflection coefficient measurement. The solid curves show pessimistic estimation of worst-case errors. The other two curves correspond to the optimistic estimation.

Figure 7 a) Measured magnitude and phase vs. frequency of an experimental iris-coupled short-circuited waveguide. (b) Smith chart display of the impedance characteristic of the experimental cavity near resonance.

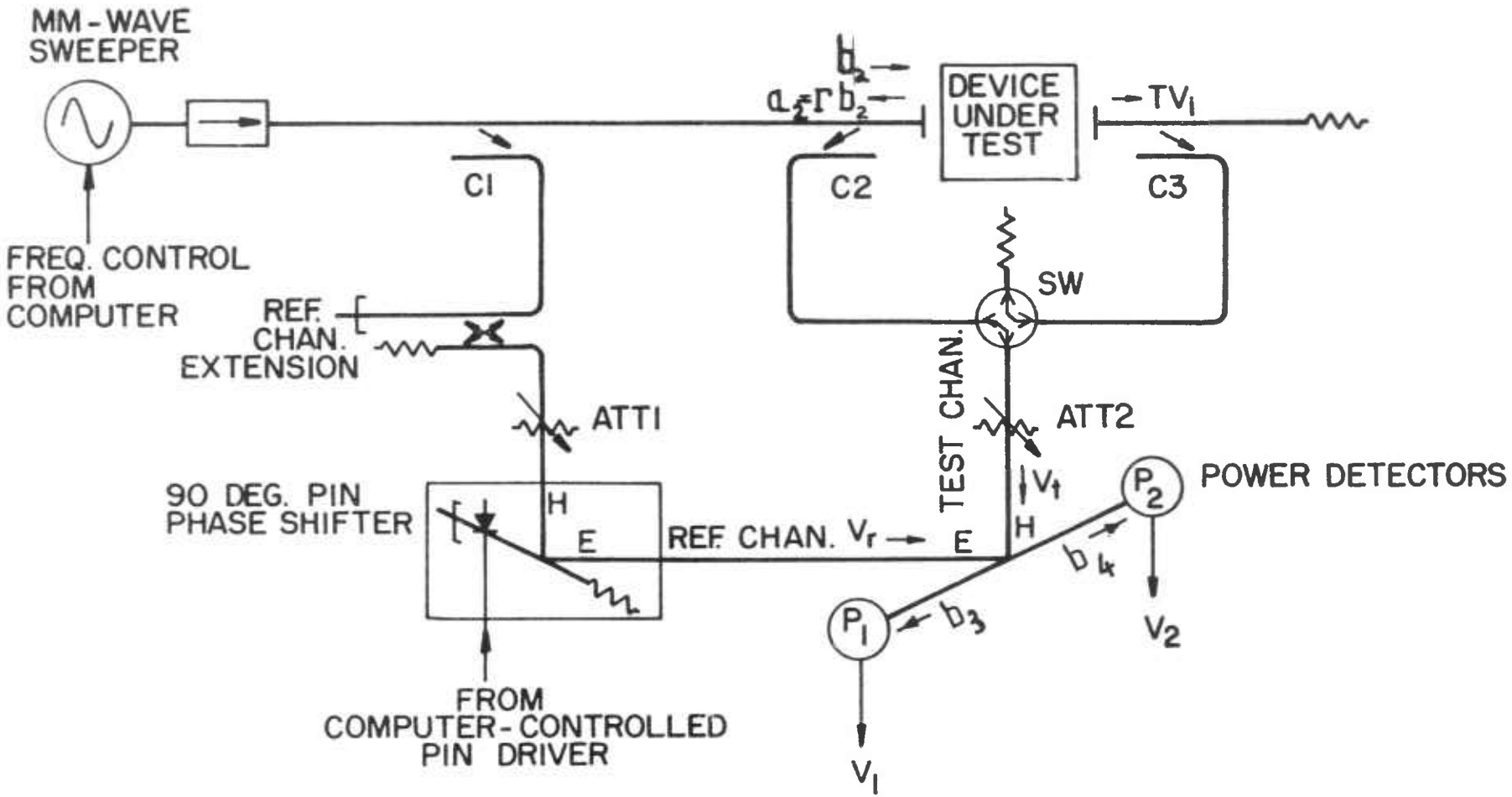

MM-WAVE SWEEPER
FREQ. CONTROL FROM COMPUTER
C1
REF. CHAN. EXTENSION
ATT1
90 DEG. PIN PHASE SHIFTER
H
E
FROM COMPUTER-CONTROLLED PIN DRIVER
REF. CHAN. V_r
$a_2 = \Gamma b_2$
b_2
DEVICE UNDER TEST
TV_1
C2
C3
SW
TEST CHAN.
ATT2
V_1
P_2
POWER DETECTORS
b_4
V_2
P_1
b_3
V_1

FIGURE 1

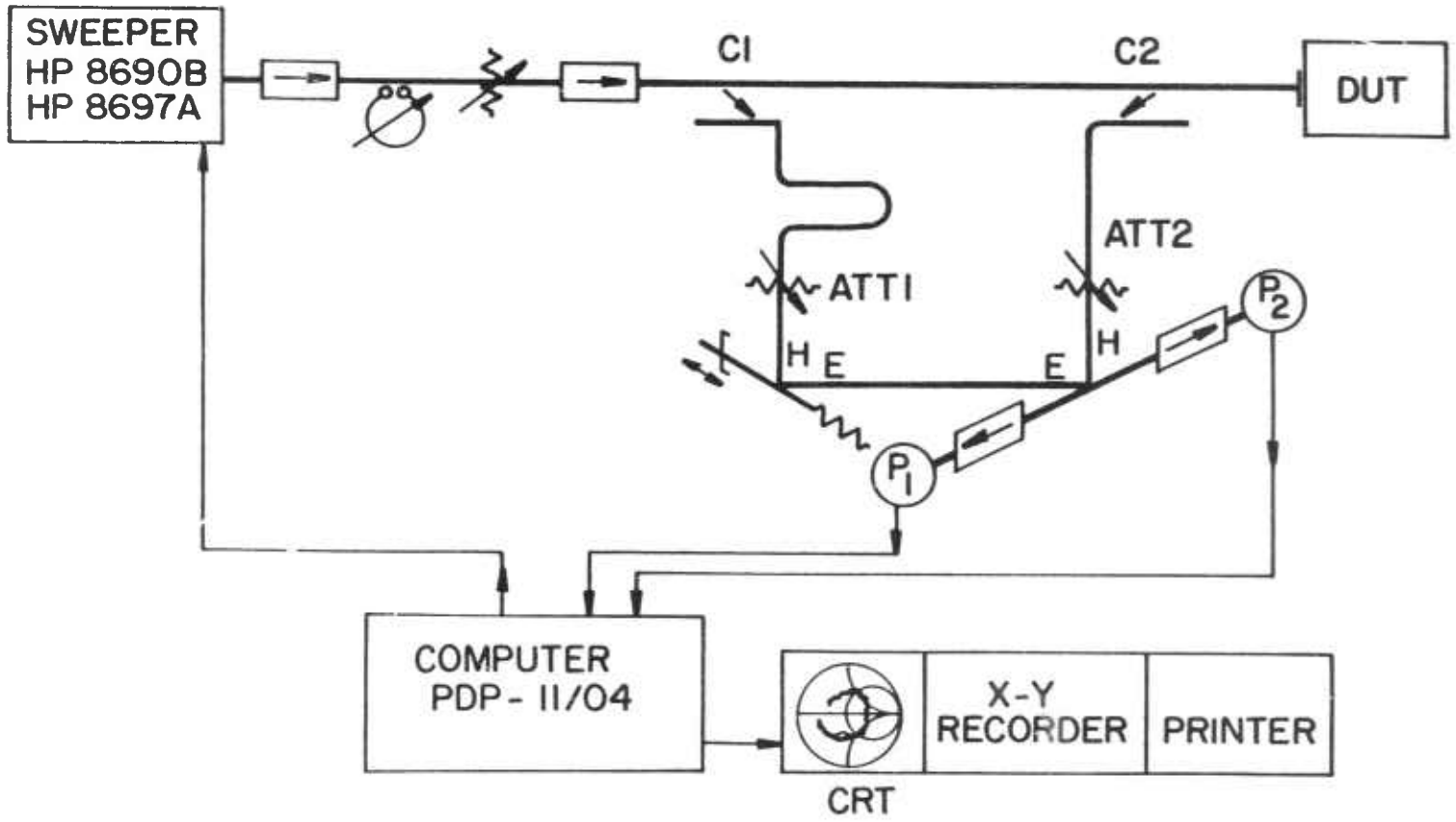

SWEEPER
HP 8690B
HP 8697A
C1
C2
DUT
ATT1
ATT2
H E
E H
P1
P2
COMPUTER
PDP-11/04
CRT
X-Y
RECORDER
PRINTER

FIGURE 2

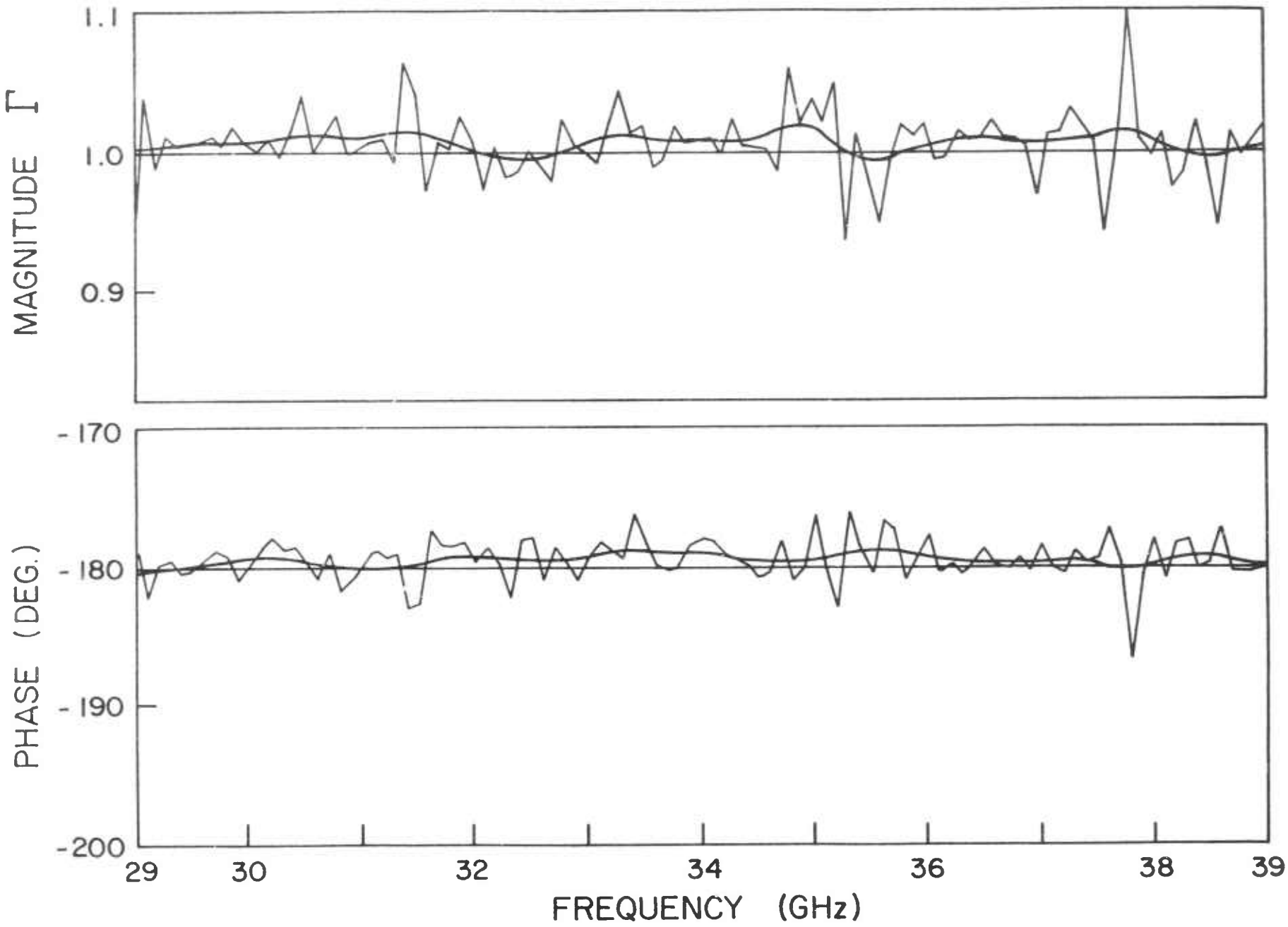

1.1
1.0
0.9
MAGNITUDE Γ
-170
-180
-190
-200
PHASE (DEG.)
29
30
32
34
36
38
39
FREQUENCY (GHz)

FIGURE 3a

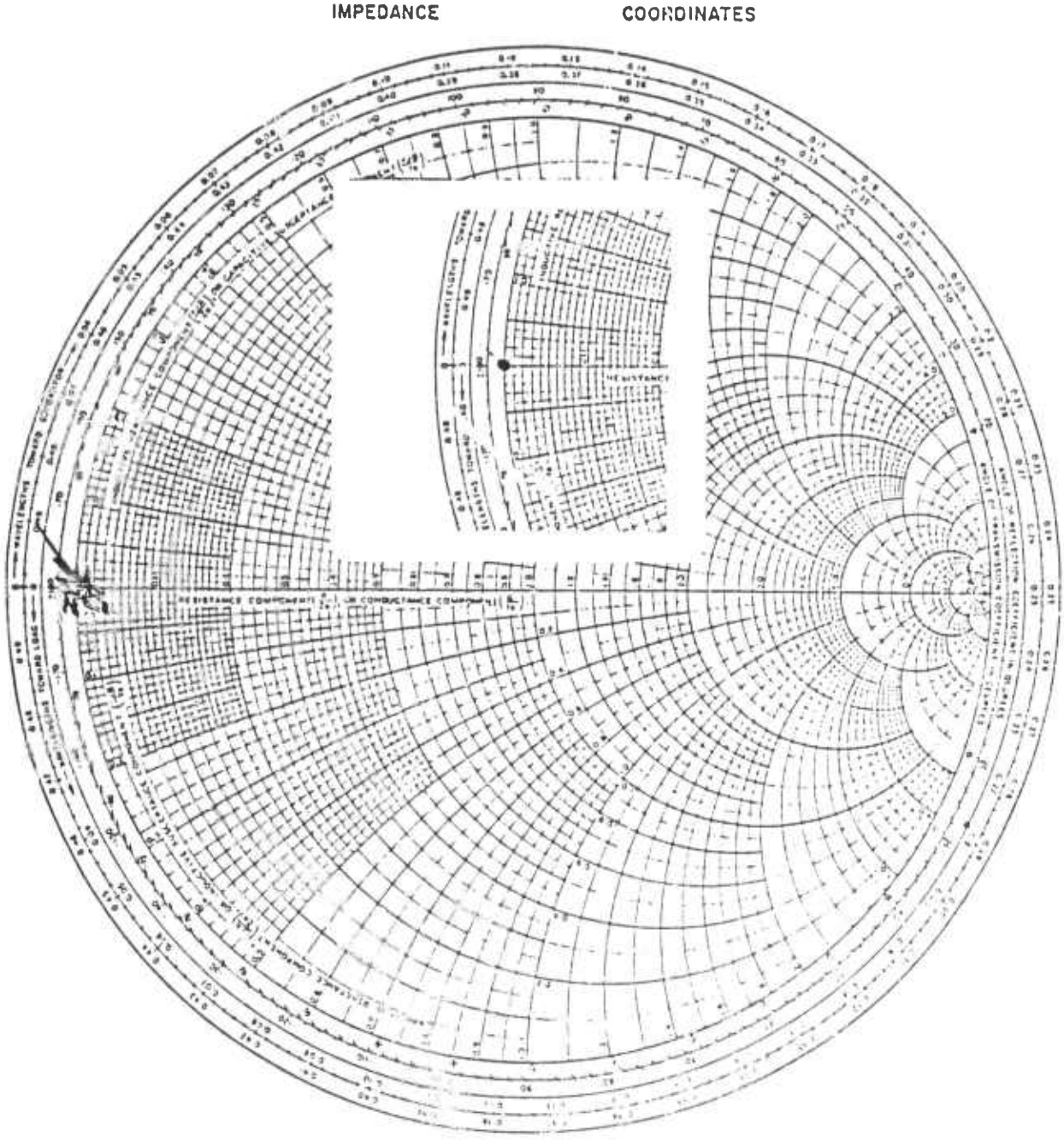


FIGURE 3b

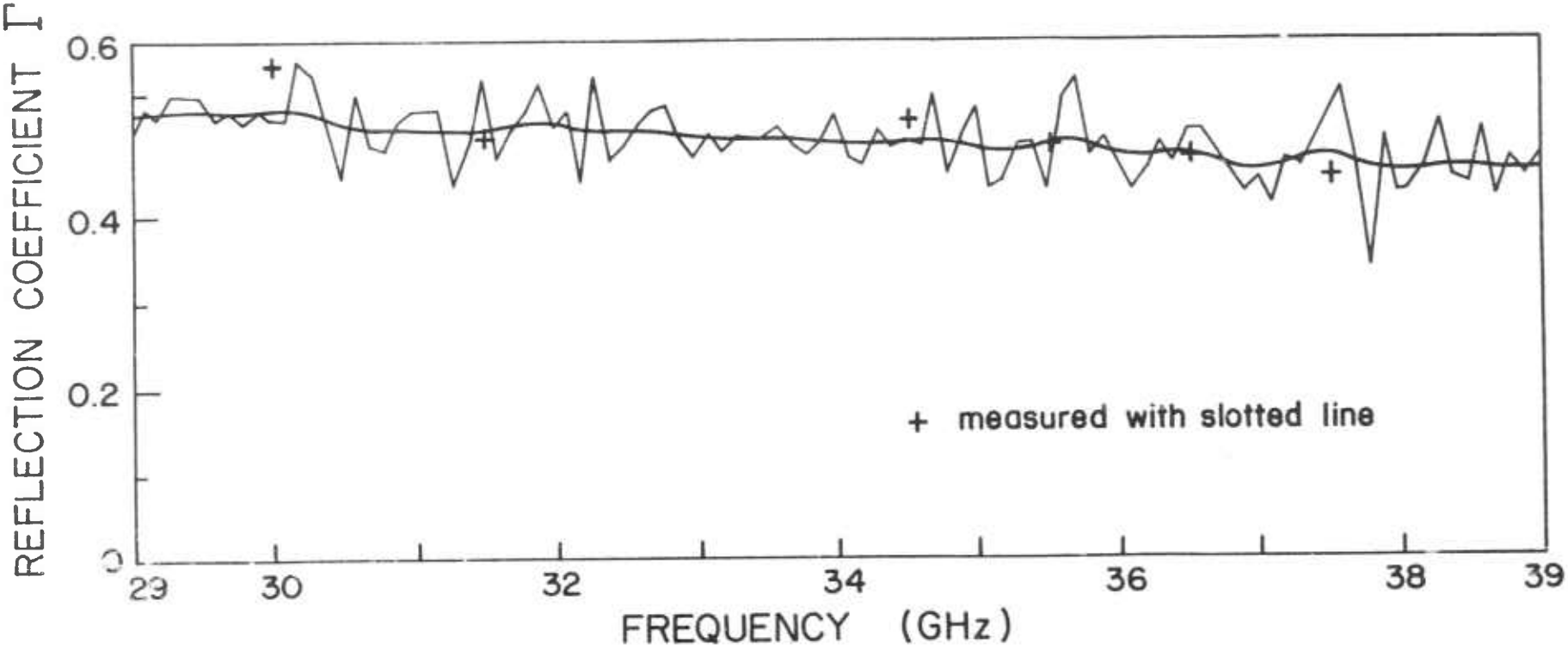

REFLECTION COEFFICIENT Γ
0.6
0.4
0.2
0
29
30
32
34
36
38
39
FREQUENCY (GHz)
+ measured with slotted line

FIGURE 4a

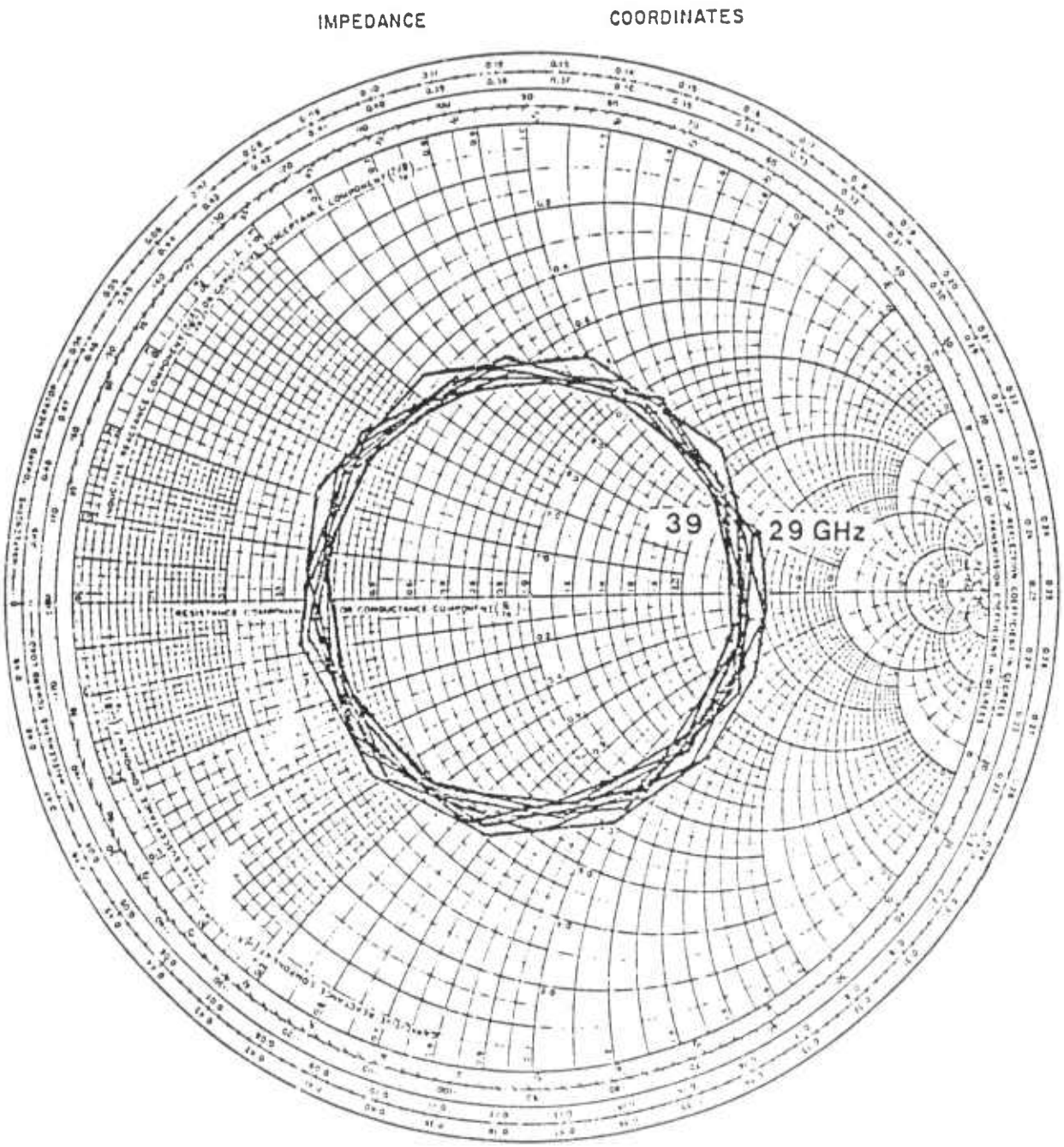


FIGURE 4b

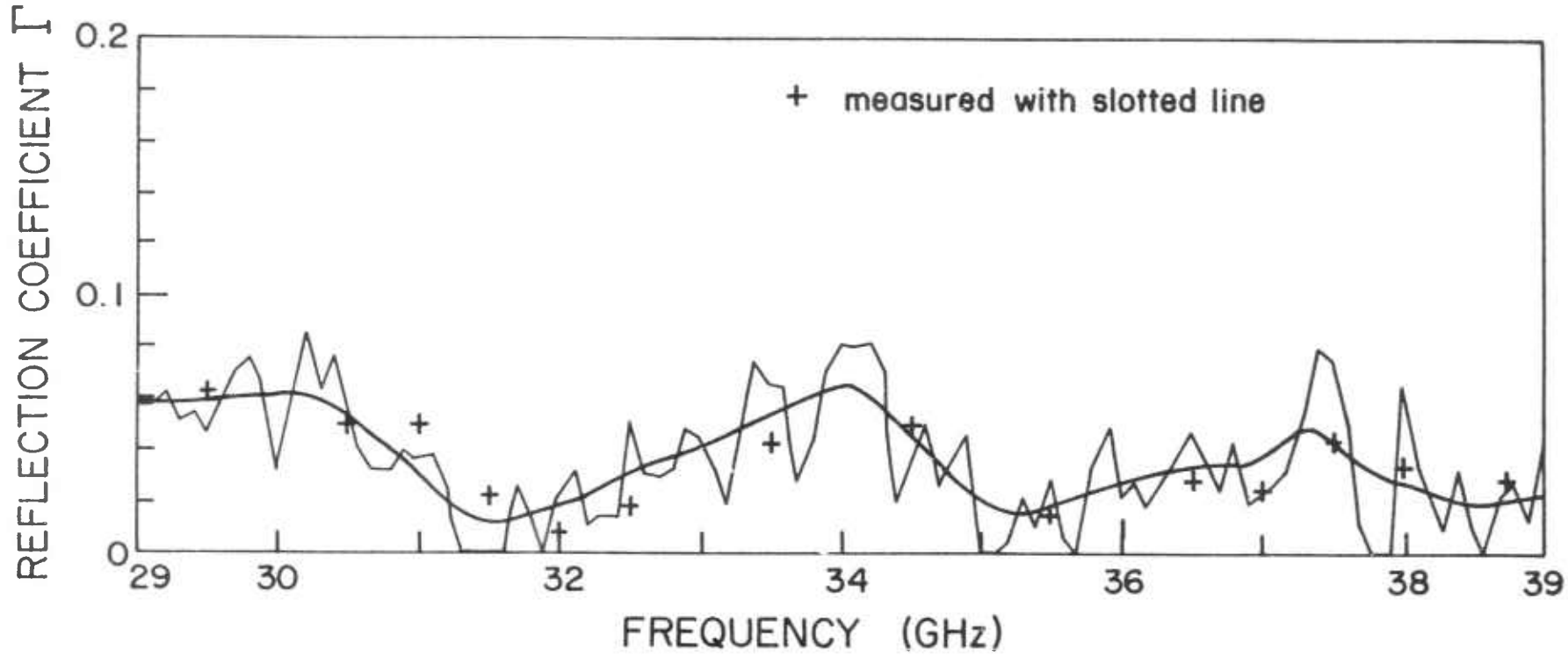

REFLECTION COEFFICIENT Γ
0.2
0.1
0
+ measured with slotted line
29
30
32
34
36
38
39
FREQUENCY (GHz)

FIGURE 5

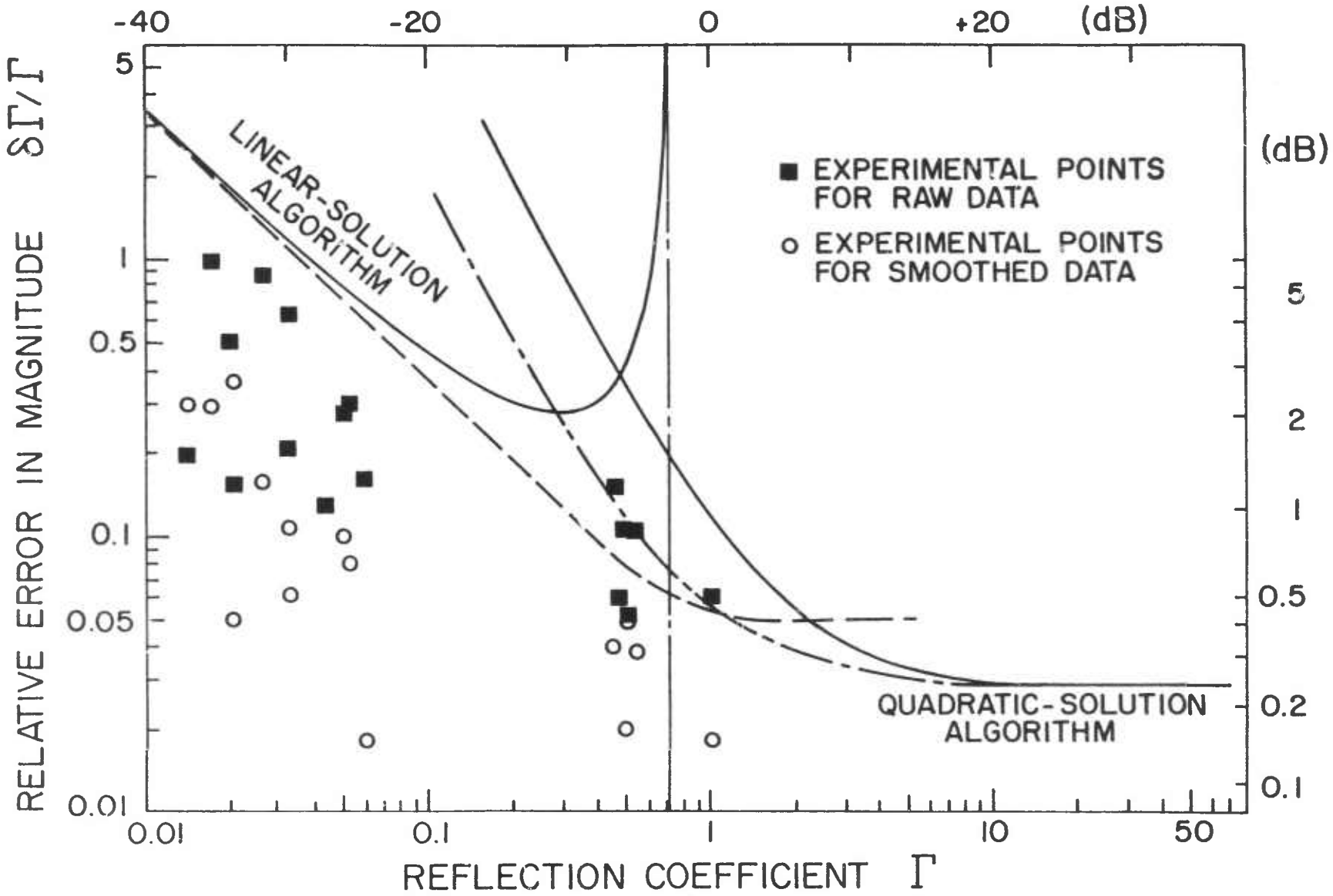

-40
-20
0
+20
(dB)
5
1
0.5
0.1
0.05
0.01
RELATIVE ERROR IN MAGNITUDE δΓ/Γ
LINEAR-SOLUTION ALGORITHM
EXPERIMENTAL POINTS FOR RAW DATA
EXPERIMENTAL POINTS FOR SMOOTHED DATA
QUADRATIC-SOLUTION ALGORITHM
(dB)
5
2
1
0.5
0.2
0.1
0.01
0.1
1
10
50
REFLECTION COEFFICIENT Γ

FIGURE 6

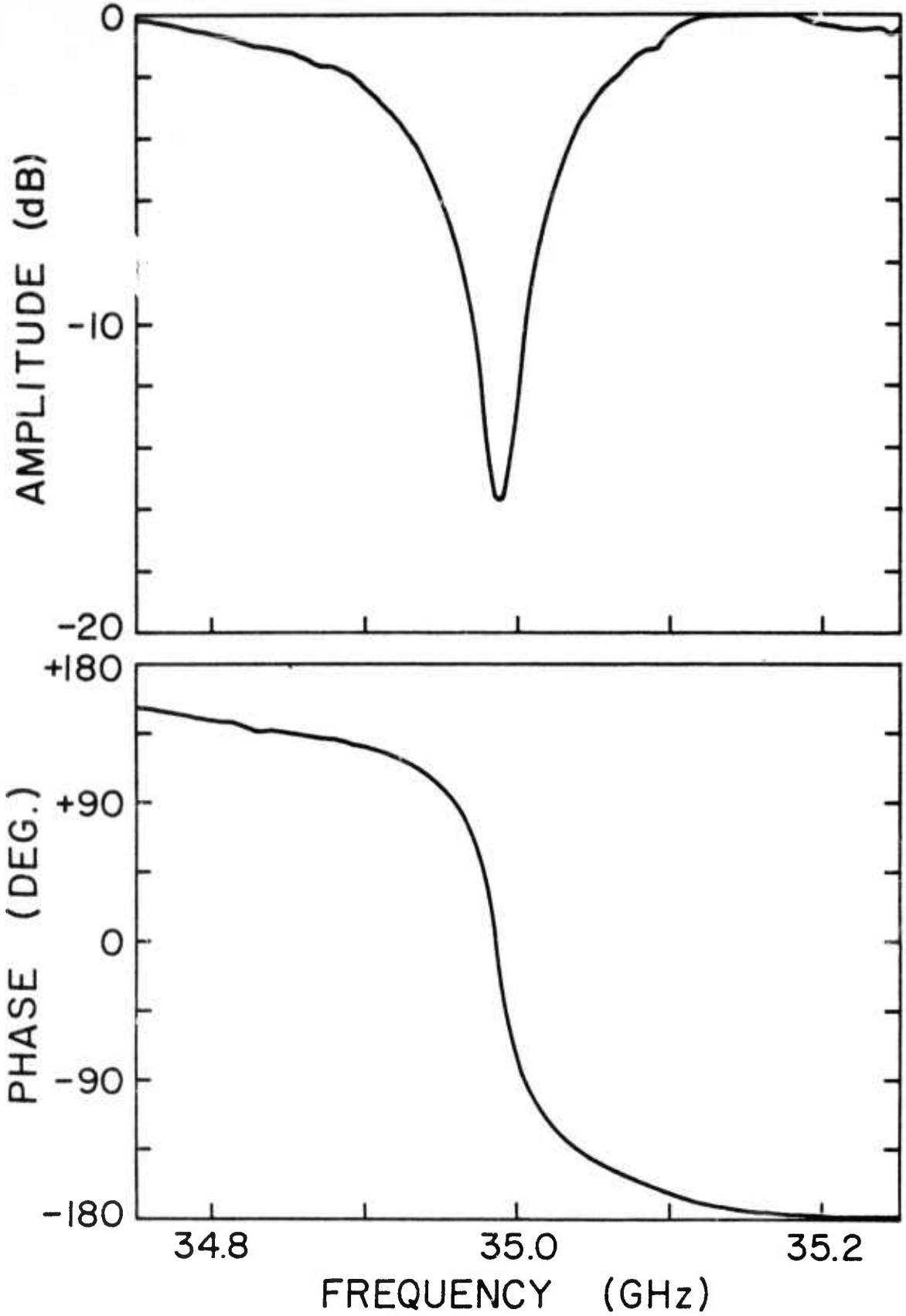

0
-10
-20
AMPLITUDE (dB)
+180
+90
0
-90
-180
PHASE (DEG.)
34.8
35.0
35.2
FREQUENCY (GHz)

FIGURE 7a

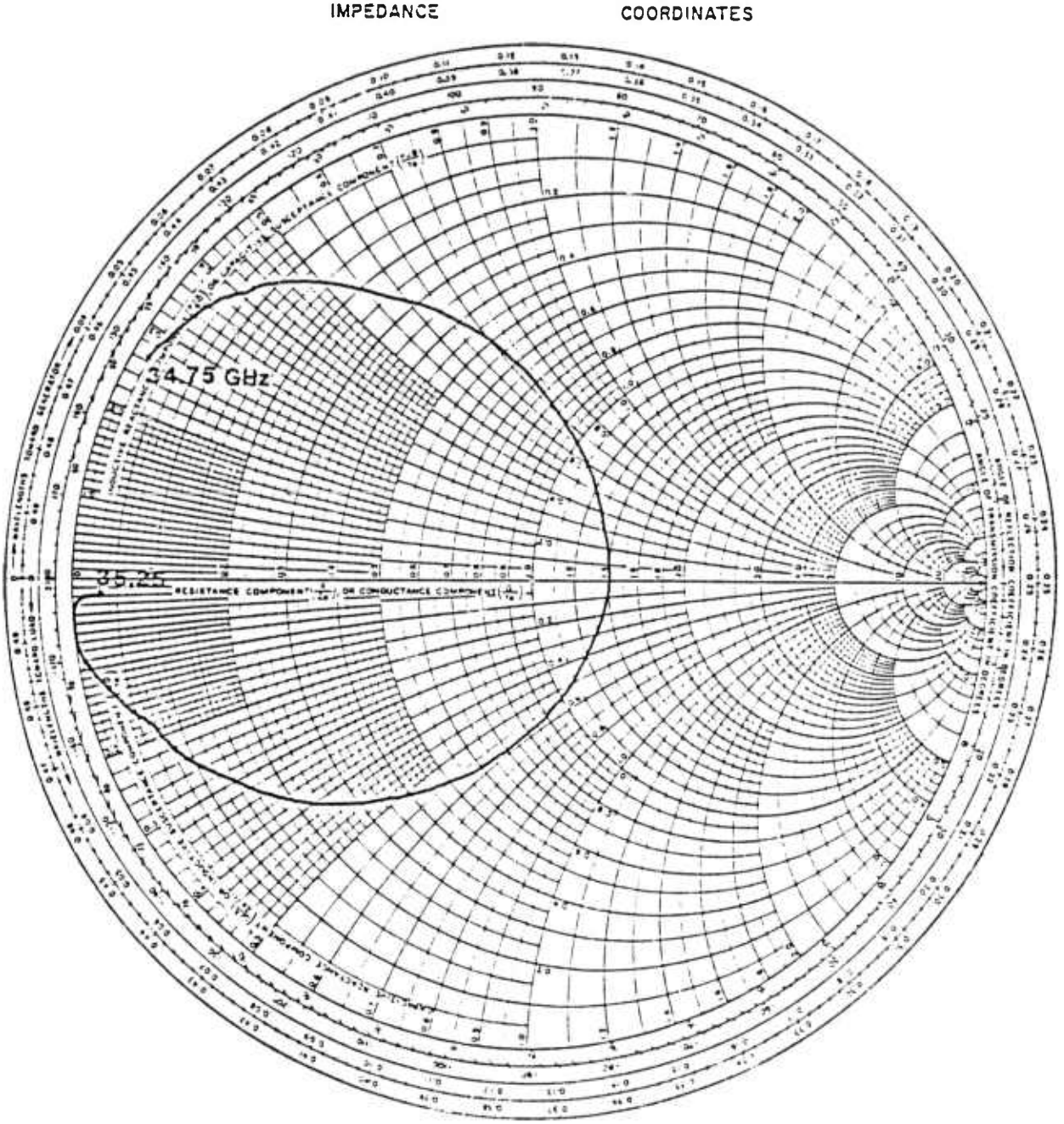


FIGURE 7b